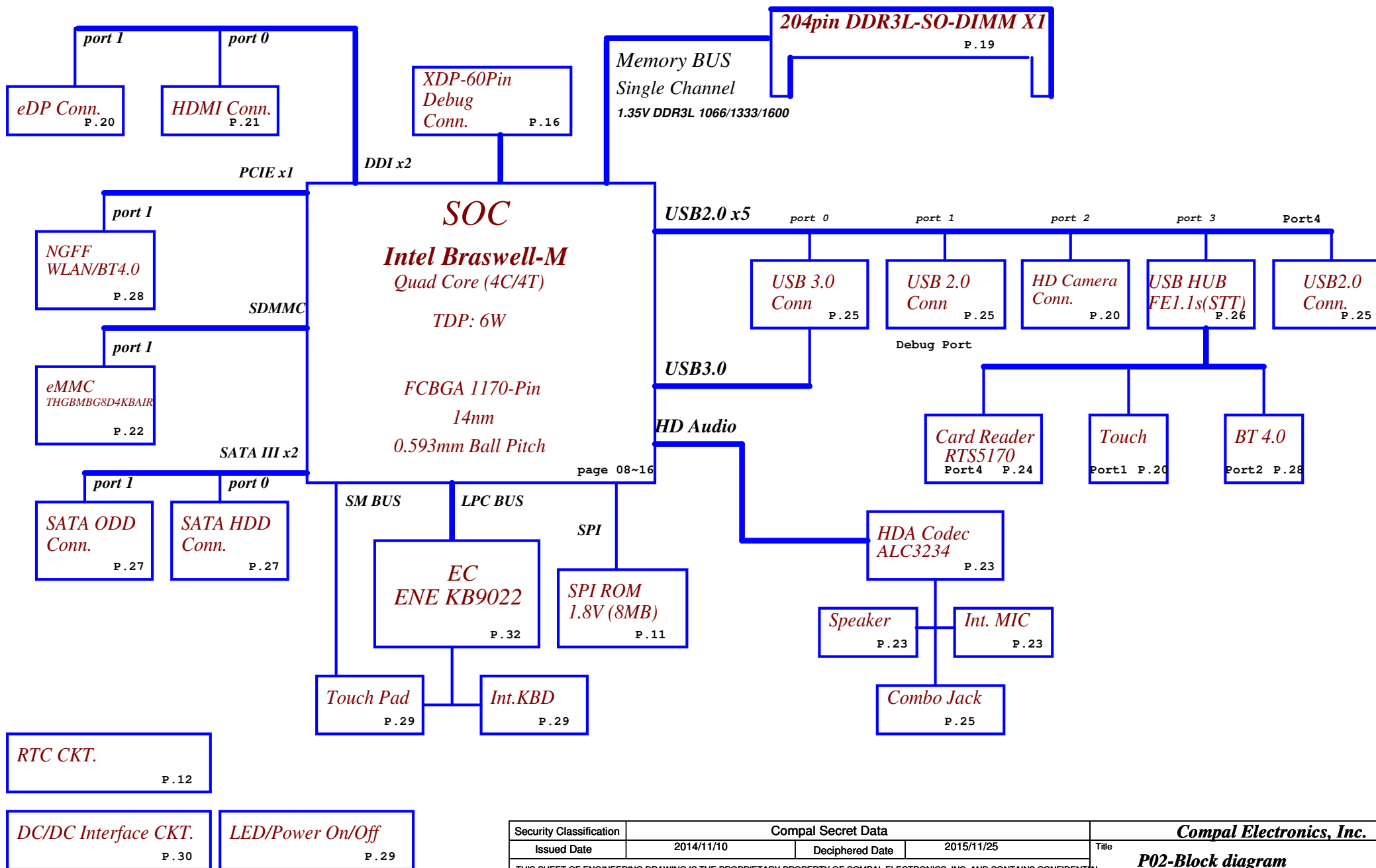


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Schematic Document  
Intel Braswell M  
UMA

2015-6-09      Rev: 1.0

ZZZ PCB®  
PCB 1EE LA-C571P REV1 M/B 2  
DA6001DX010

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## Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VALW	+1.05v Always power rail	ON	ON	ON
+1.24VALW	+1.24v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+3V_SOC	+3V_SOC Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+VCC_CORE	Core voltage for SOC	ON	OFF	OFF
+VGG_CORE	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.15VALW	+1.15VALW system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

## Board ID / SKU ID Table for AD channel

Board ID Table for AD channel

Vcc	3.3V +/- 1%						
Ra	100K +/- 1%						
Board ID	Rb	VAD_BID_min	VAD_BID_typ	VAD_BID_max	EC_AD3		
0	0	0.000V	0.000V	0.300V	0x00 -	0x0B	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C -	0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D -	0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 -	0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 -	0x3B	
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C -	0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 -	0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 -	0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 -	0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 -	0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 -	0x96	
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 -	0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 -	0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE -	0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 -	0xC0	
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 -	0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA -	0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 -	0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD -	0xEE	
19	NC	3.000V	3.300V	3.300V	0xEF -	0xFF	

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0

## BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMI@
EMC requirement unpop	NEMI@
LPC18	LPC18@
LPC33	LPC33@
Rvs. RF requirement	RF@
ESD requirement	ESD@
XDP (Debug Port) unpop	NXDP@
ESD requirement unpop	NESD@
For JUMP	JP@
For PCB	PCB@
For CPU	SOC@ SOC1@
SATA re-Driver	601@
Test Point	TP@
SATA re-Driver unpop	N601@

## 43 level BOM table

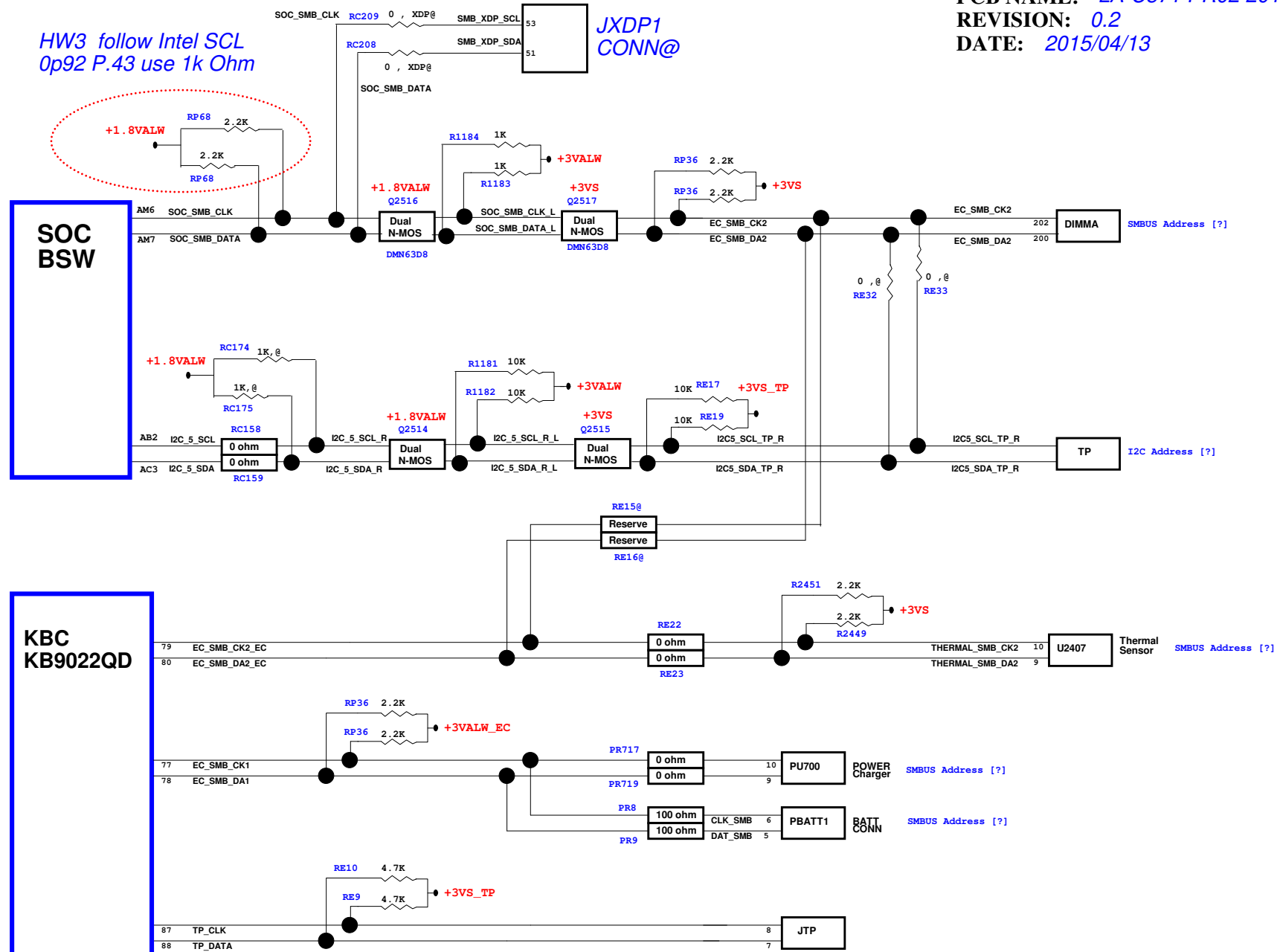
43 Level	Description	BOM Structure
4319Y031L01	MB AC571 AAL14 BSW U PEN HDMI	EMI@/ESD@/XDP@/LPC33@/PCB@/ODD@/SOC@/601@/N601@/PARADE@
4319Y031L02	MB AC571 AAL14 BSW U CEL HDMI	EMI@/ESD@/XDP@/LPC33@/PCB@/ODD@/SOC1@/601@/N601@/PARADE@

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				B	LA-C571P	1.0
				Date:	Tuesday, June 16, 2015	Sheet 4 of 44

MODEL NAME: *SMBus Block Diagram*  
PCB NAME: *LA-C571 PR02 2015/03/27*  
REVISION: *0.2*  
DATE: *2015/04/13*

*HW3 follow Intel SCL  
Op92 P.43 use 1k Ohm*

*JXDP1  
CONN@*

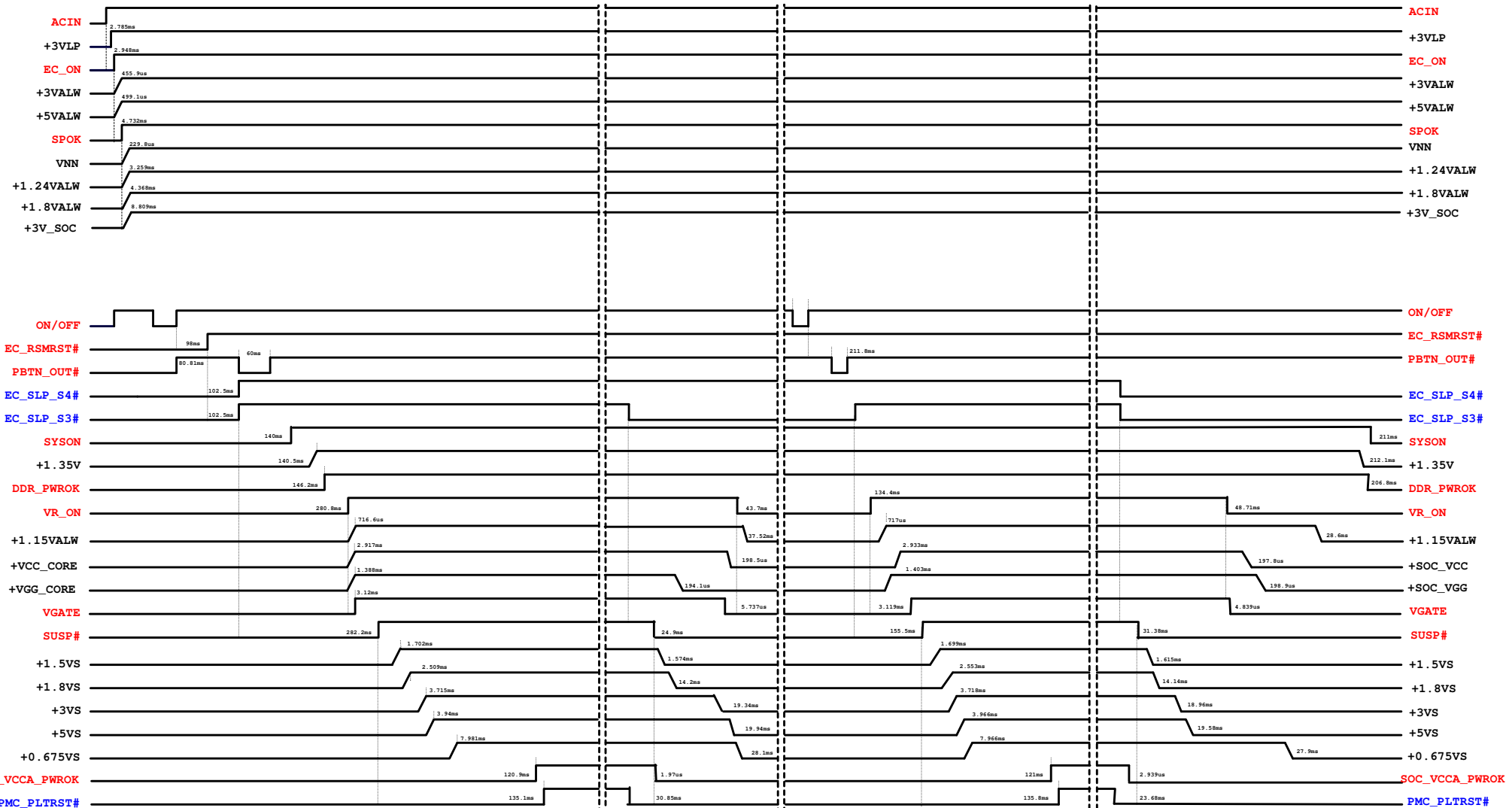


S5-&gt;S0

S0-&gt;S3

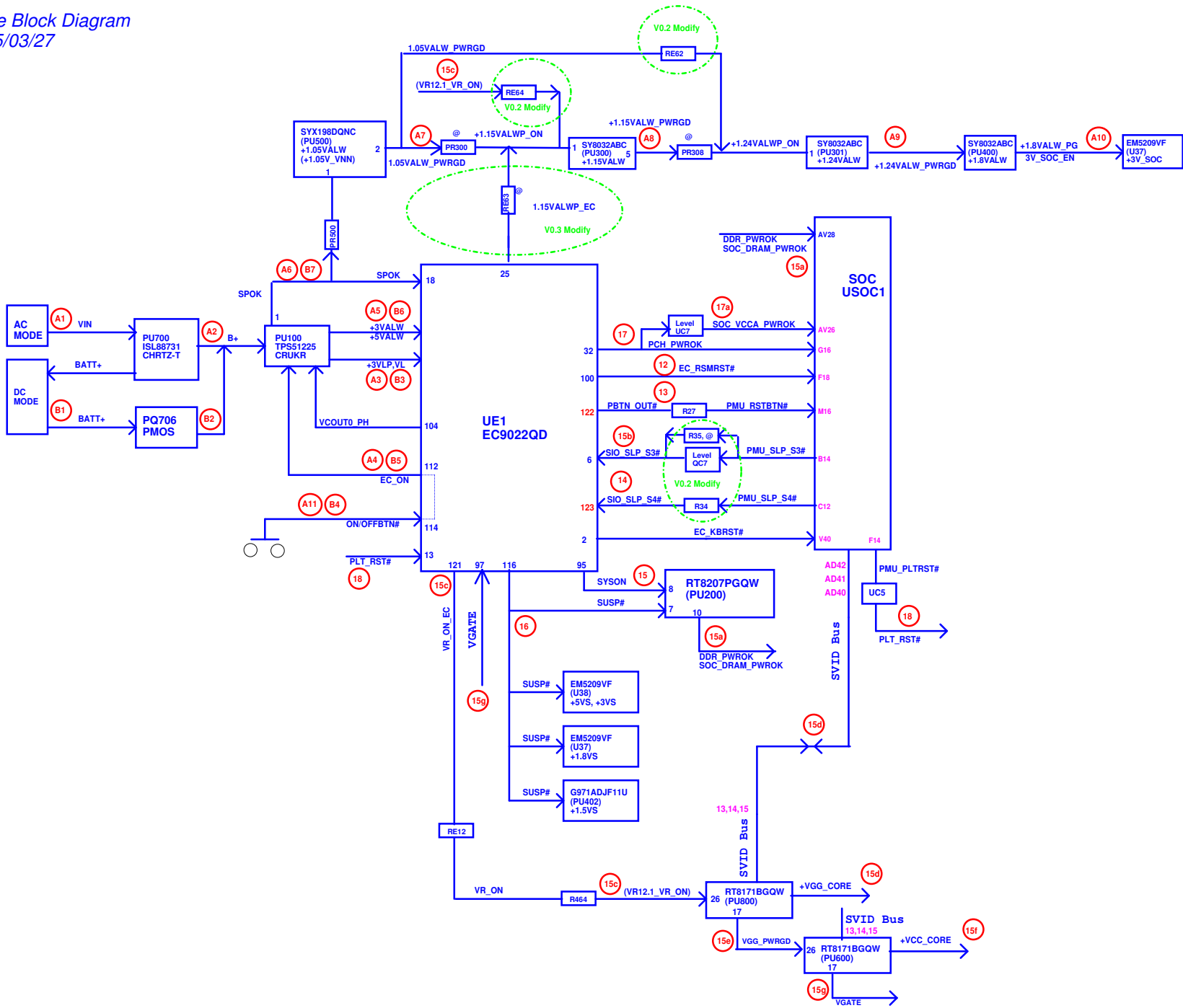
S3-&gt;S0

S0-&gt;S5



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					Document Number LA-C571P
					Rev 1.0
					Date: Tuesday, June 16, 2015
					Sheet 6 of 44

MODEL NAME: Power Sequence Block Diagram  
PCB NAME: LA-C571PR02 2015/03/27  
REVISION: 0.2  
DATE: 2015/04/13



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				LA-C571P	1.0
				Date: Tuesday, June 16, 2015	Sheet 7 of 44

Main Func = CPU

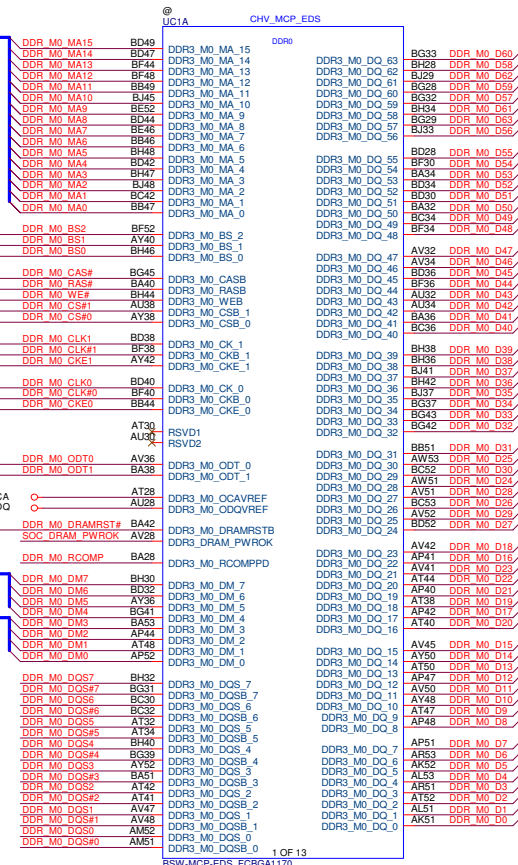
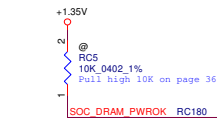
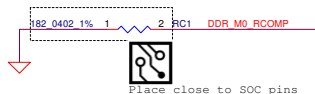
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SOC@

S IC A31 FH806501715906 QJMS C0 1.6G  
Part Number = SA00008U52L

UC1  
SOC@

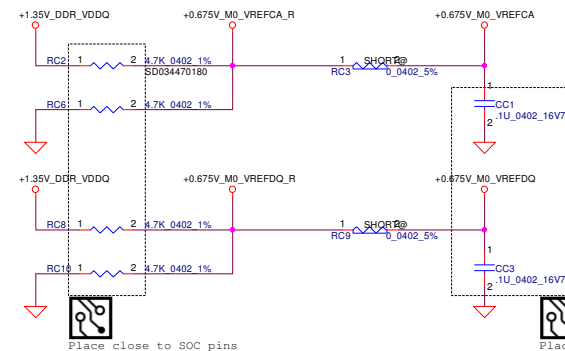
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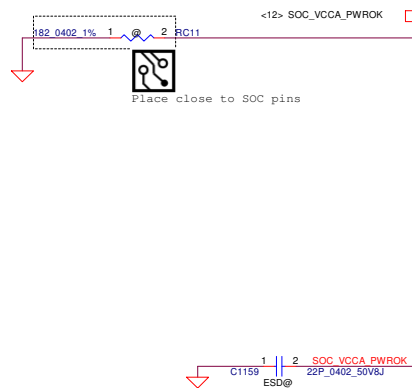
Power Name and Connection Check OK

8 mils minimum for maximum of 300 mils in breakout area



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Main Func = CPU



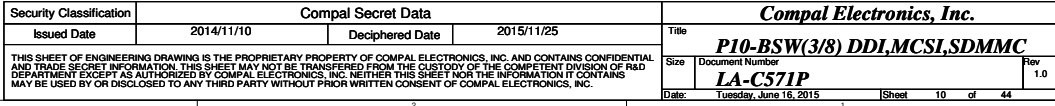
CHV_MCP_EDS		
UC1B	DOR1	
BD5	DDR3_M1_MA_15	BG21
BD7	DDR3_M1_MA_14	BH26
BF10	DDR3_M1_MA_13	BH25
BB5	DDR3_M1_MA_12	BG26
BJ8	DDR3_M1_MA_11	BG22
BE2	DDR3_M1_MA_10	BH20
BD10	DDR3_M1_MA_9	BG25
BE8	DDR3_M1_MA_8	BH21
BB8	DDR3_M1_MA_7	
BH8	DDR3_M1_MA_6	BD26
BD12	DDR3_M1_MA_5	BF24
BH12	DDR3_M1_MA_4	BA20
BJ6	DDR3_M1_MA_3	BD20
BC12	DDR3_M1_MA_2	BD24
BE1	DDR3_M1_MA_1	BA22
	DDR3_M1_MA_0	BA18
BF2	DDR3_M1_BS_2	BF20
AY18	DDR3_M1_BS_1	
BH1	DDR3_M1_BS_0	AV22
		AV20
BC9	DDR3_M1_CASB	BD18
BA18	DDR3_M1_RASB	BF18
BH10	DDR3_M1_WEB	AU22
AU18	DDR3_M1_CSB_1	AU20
AY18	DDR3_M1_CSB_0	BA18
		BC18
BD18	DDR3_M1_CK_1	
BF18	DDR3_M1_CKB_1	BH18
AY12	DDR3_M1_CKE_1	BJ13
		BH12
BD14	DDR3_M1_CK_0	BJ17
BF10	DDR3_M1_CKB_0	BG17
BB10	DDR3_M1_CKE_0	BG11
AT24		BD12
AU24	RSVD1	
	RSVD2	BB3
AV18	DDR3_M1_DQ_31	BW1
BA18	DDR3_M1_DQ_30	BC2
	DDR3_M1_ODT_1	AW3
AT28	DDR3_M1_OCAVREF	AV3
AU28	DDR3_M1_ODQVREF	BC1
BA12	DDR3_M1_DRAMRSTB	AV2
AY28	DDR3_VCCA_PWROK	BD2
BA26	DDR3_M1_RCOMP	AV12
		AP13
BH24	DDR3_M1_DM_7	AV13
BD22	DDR3_M1_DM_6	AT10
AY18	DDR3_M1_DM_5	AP14
BG14	DDR3_M1_DM_4	AT16
BA1	DDR3_M1_DM_3	AT14
AP10	DDR3_M1_DM_2	
AT8	DDR3_M1_DM_1	AV9
AP2	DDR3_M1_DM_0	AV4
		AT14
BH22	DDR3_M1_DQS_7	AP7
BG22	DDR3_M1_DQS_6	AV4
BC22	DDR3_M1_DQS_5	AV6
AT22	DDR3_M1_DQS_4	AT7
BH18	DDR3_M1_DQS_3	AP6
BG18	DDR3_M1_DQS_2	
AY2	DDR3_M1_DQS_1	AP3
BA3	DDR3_M1_DQS_0	BR1
AT12	DDR3_M1_DQSB_3	AK2
AT12	DDR3_M1_DQSB_2	AL1
AV2	DDR3_M1_DQSB_1	BR3
AM2	DDR3_M1_DQSB_0	AT2
AM2		AL3
		AK3

2 OF 13

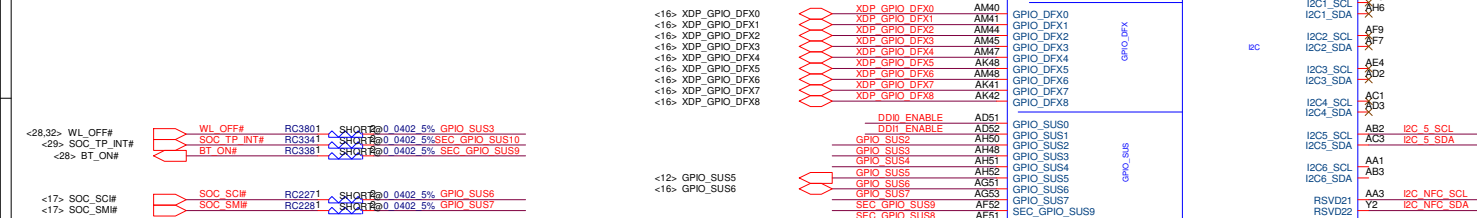
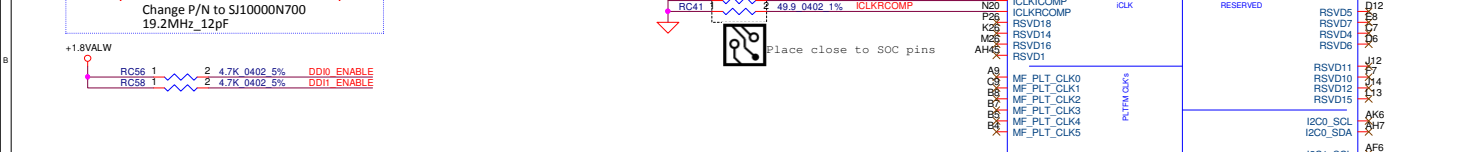
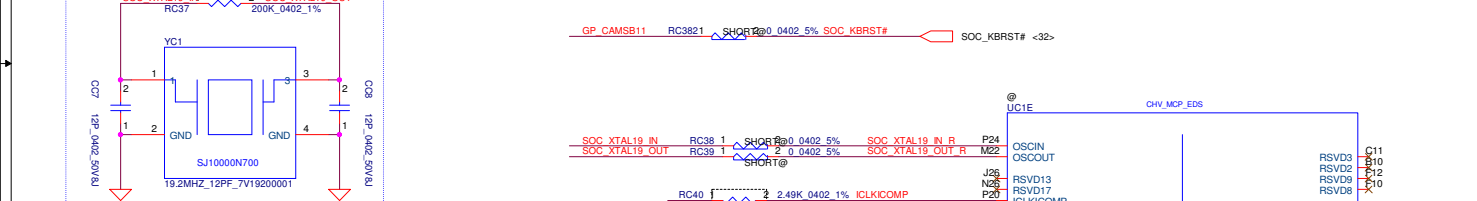
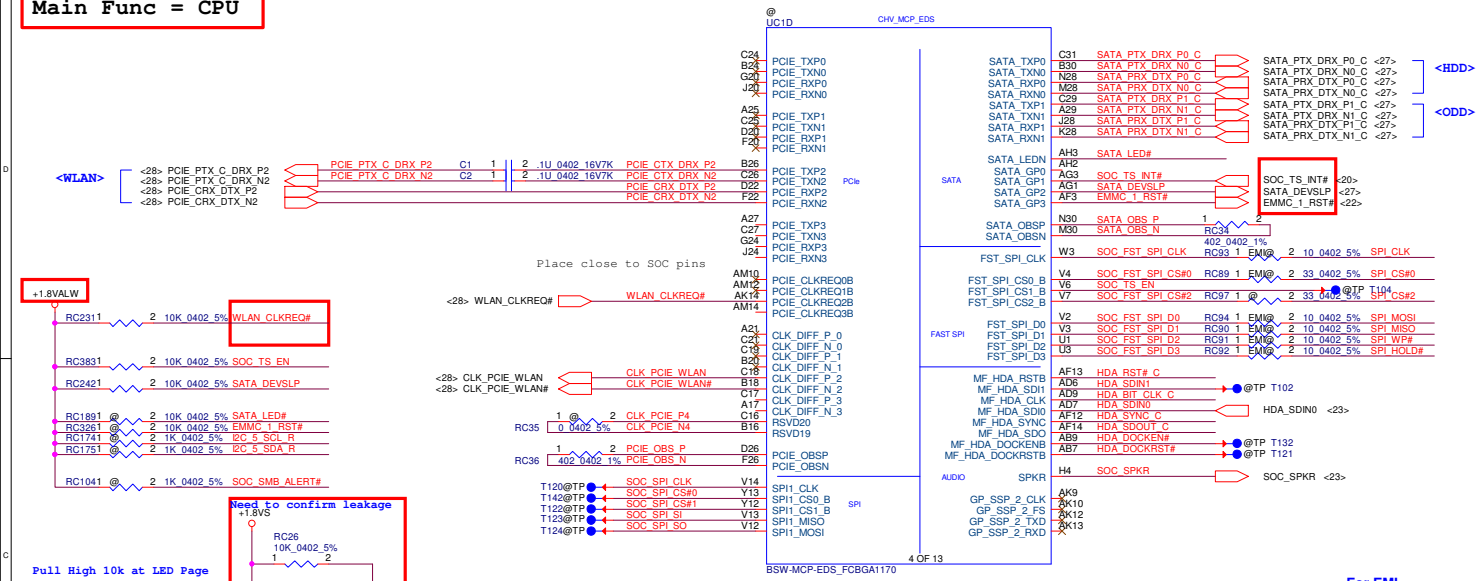
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				Sheet	9 of 44

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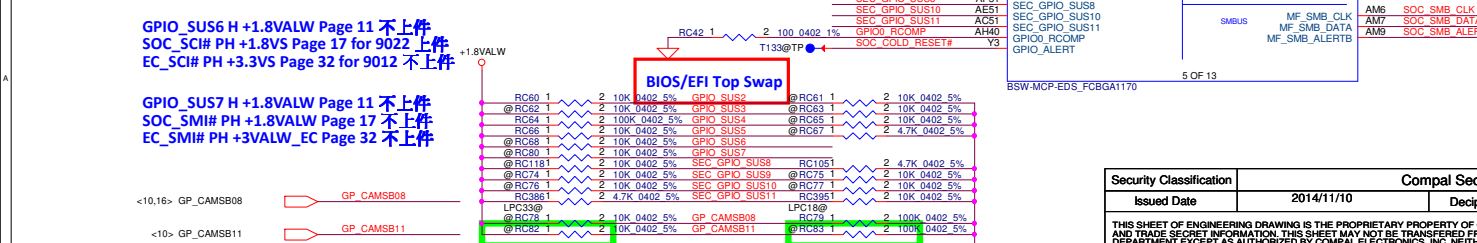


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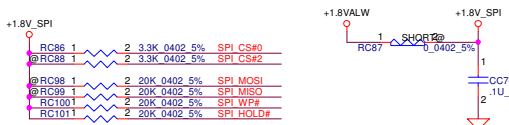


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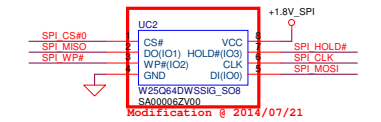
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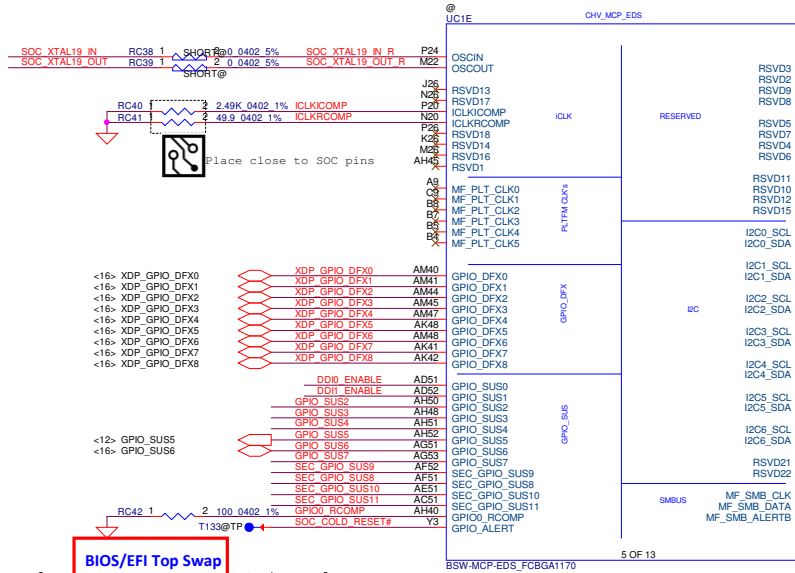
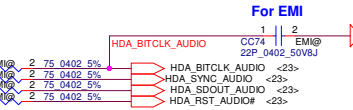
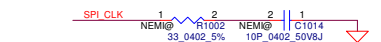
## BIOS ROM



SPI ROM ( 8MByte/1.8V/Quad-IO )



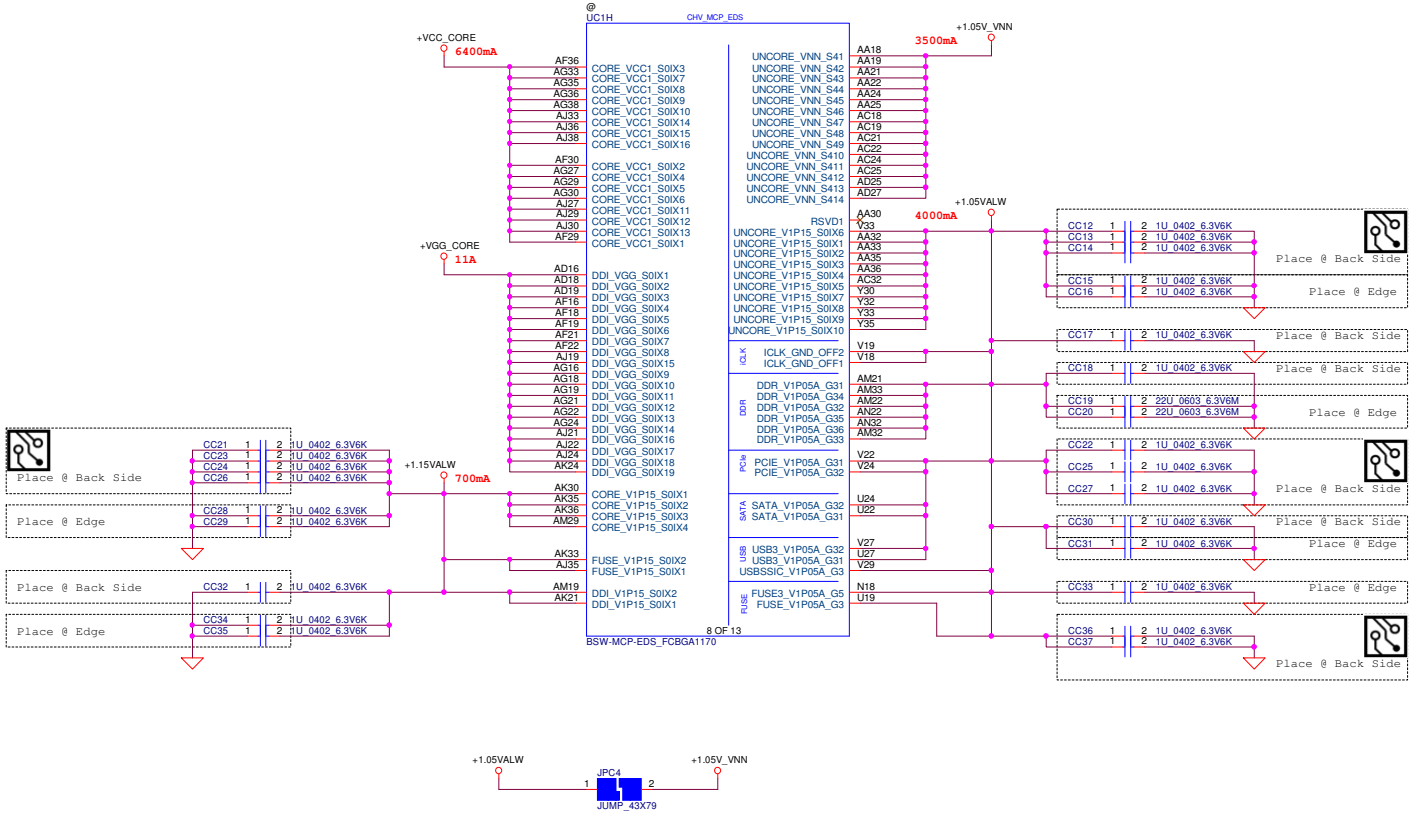
Reserve for EMI(Near SPI ROM)



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				Date:	Tuesday, June 16, 2015	Sheet

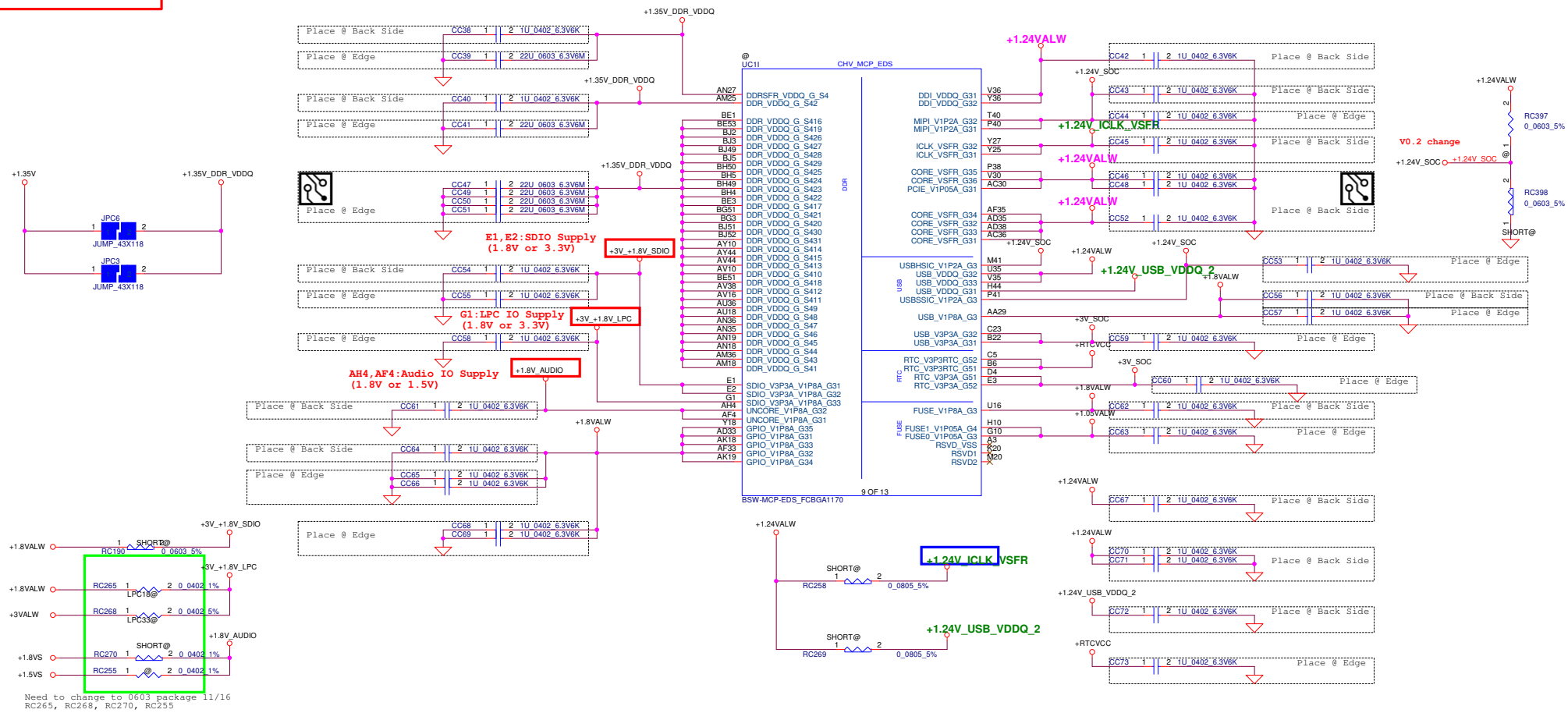


Main Func = CPU



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				Date:	Tuesday, June 16, 2015	Sheet 13 of 44

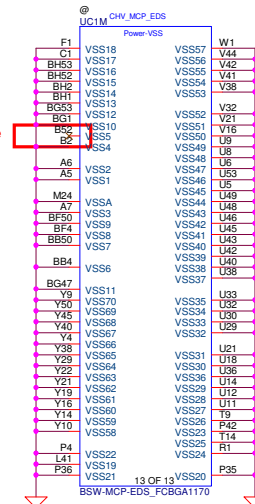
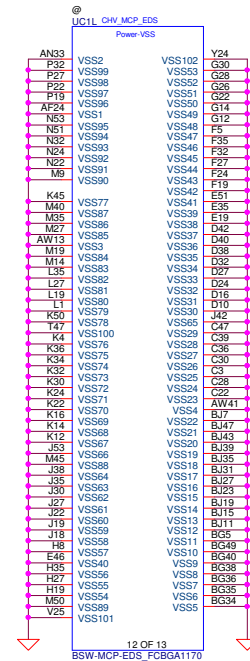
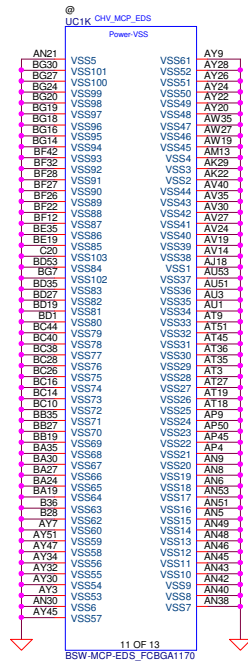
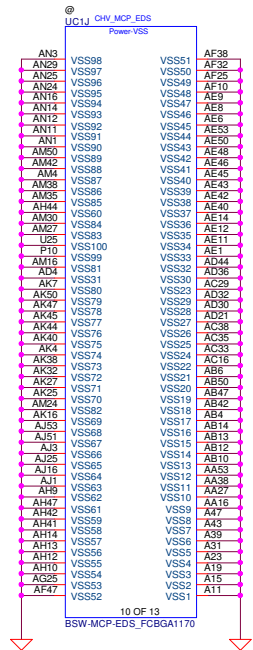
Main Func = CPU



NOTE:  
+1.24V\_MIPI, +1.24V\_USBHSIC, +1.24V\_USBSIC are +1.24V Only.  
[PDG Rev0p92 P.55]  
When SSIC, HSIC & CSI interface is not used, the following pins can be connected to ground:  
CSI (T40, P40), USB HSIC (M41), USB SSIC (P41).

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				LA-C571P	Rev 1.0
				Date	Tuesday, June 16, 2015
				Sheet	14 of 44

**Main Func = CPU**

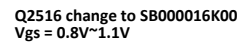


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Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	P15-BSW(8/8) GND	
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					LA-C571P	1.0
				Date:	Tuesday, June 16, 2015	Sheet 15 of 44

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Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title <b>P16-Intel Debug</b>	
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				Document Number	1.0
				Date	Tuesday, June 16, 2015
				Sheet	16 of 44

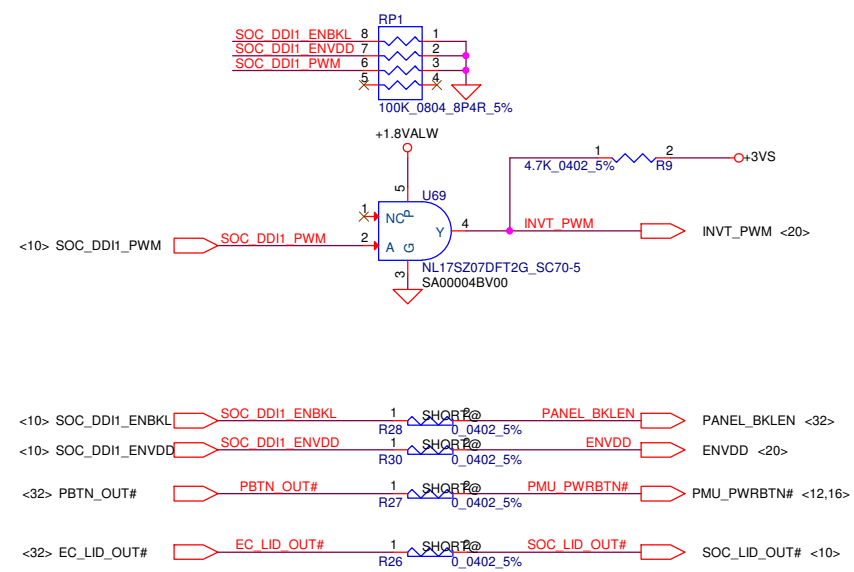
## POWER ON SEQUENCE



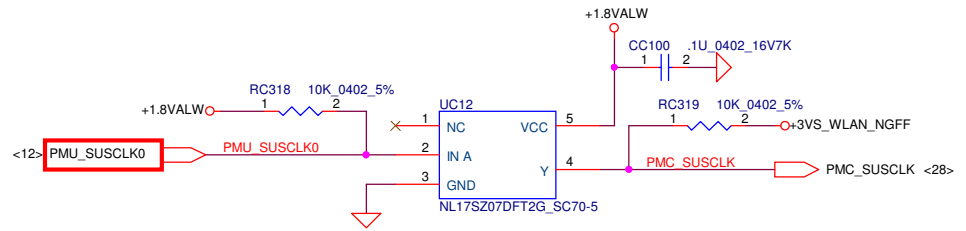
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/11/10	Deciphered Date	2015/11/25	Title	P17-Level Shift-1	
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					LA-CS71P	1.0
				Date:	Tuesday, June 16, 2015	Sheet 17 of 44

Main Func = Level Shift

eDP Control



WLAN



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Main Func = DIMM

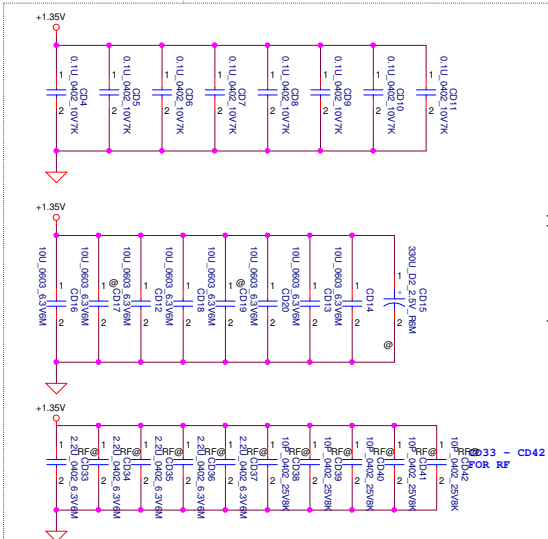
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1  
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

<8> DDR\_M0\_DM[4,7]  
<8> DDR\_M0\_DM[0,3]  
<8> DDR\_M0\_DQS[0,7]  
<8> DDR\_M0\_DQS[0,7]  
<8> DDR\_M0\_DQ[0,31]  
<8> DDR\_M0\_DQ[32,63]  
<8> DDR\_M0\_MA[0,15]

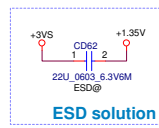
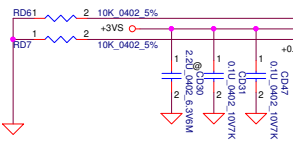
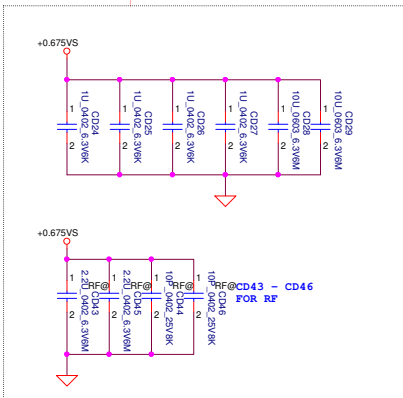
All VREF traces should have 10 mil trace width

Layout Note:  
Place near JDIMM1

Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket



Layout Note:  
Place near JDIMM1.203,204



<8> DDR\_M0\_CKE0  
<8> DDR\_M0\_BS2  
<8> DDR\_M0\_CLK0  
<8> DDR\_M0\_CLK#0  
<8> DDR\_M0\_BS0  
<8> DDR\_M0\_WE#  
<8> DDR\_M0\_CAS#  
<8> DDR\_M0\_CS#1

DDR\_M0\_CKE0  
DDR\_M0\_BS2  
DDR\_M0\_CLK0  
DDR\_M0\_CLK#0  
DDR\_M0\_BS0  
DDR\_M0\_WE#  
DDR\_M0\_CAS#  
DDR\_M0\_CS#1

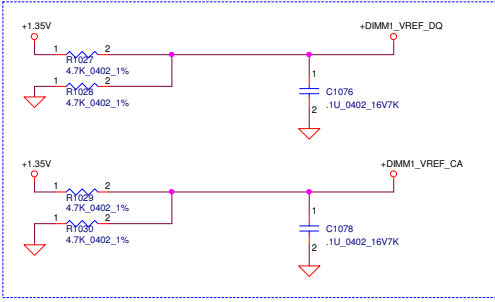
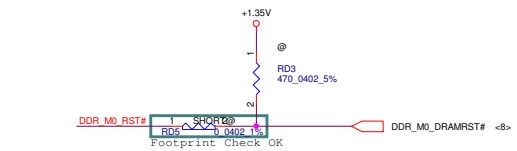
DDR\_M0\_D32  
DDR\_M0\_D33  
DDR\_M0\_DQS#4  
DDR\_M0\_DQS#4  
DDR\_M0\_D34  
DDR\_M0\_D35  
DDR\_M0\_D40  
DDR\_M0\_D41  
DDR\_M0\_DM5  
DDR\_M0\_D42  
DDR\_M0\_D43  
DDR\_M0\_D48  
DDR\_M0\_D49  
DDR\_M0\_DQS#6  
DDR\_M0\_DQS#6  
DDR\_M0\_D50  
DDR\_M0\_D51  
DDR\_M0\_D56  
DDR\_M0\_D57  
DDR\_M0\_DM7  
DDR\_M0\_D58  
DDR\_M0\_D59

DDR\_M0\_D32  
DDR\_M0\_D33  
DDR\_M0\_DQS#4  
DDR\_M0\_DQS#4  
DDR\_M0\_D34  
DDR\_M0\_D35  
DDR\_M0\_D40  
DDR\_M0\_D41  
DDR\_M0\_DM5  
DDR\_M0\_D42  
DDR\_M0\_D43  
DDR\_M0\_D48  
DDR\_M0\_D49  
DDR\_M0\_DQS#6  
DDR\_M0\_DQS#6  
DDR\_M0\_D50  
DDR\_M0\_D51  
DDR\_M0\_D56  
DDR\_M0\_D57  
DDR\_M0\_DM7  
DDR\_M0\_D58  
DDR\_M0\_D59

H=4mm

2-3A to 1 DIMMs/channel

CAD NOTE  
PLACE THE CAP NEAR TO DIMM RESET PIN



DDR\_M0\_ODT0  
DDR\_M0\_ODT1  
V0.2 change

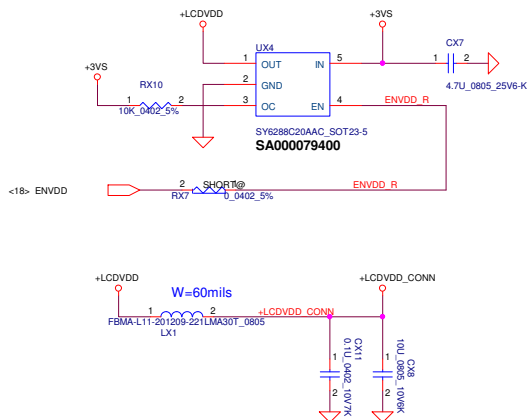
Channel A

<Address: SA1:SA0=00 (A0H)>  
DIMM\_1 STD H:4mm

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Issued Date	2014/11/10	Deciphered Date	2015/11/25	P19-DDRIII DIMMA	
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Main Func = eDP

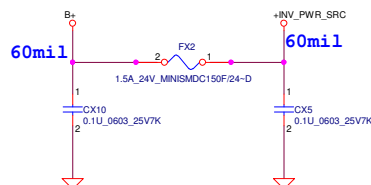
## LCD PWR CTRL



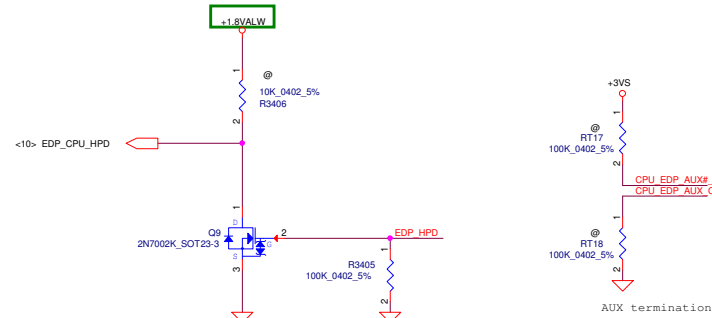
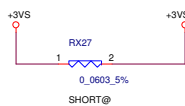
SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

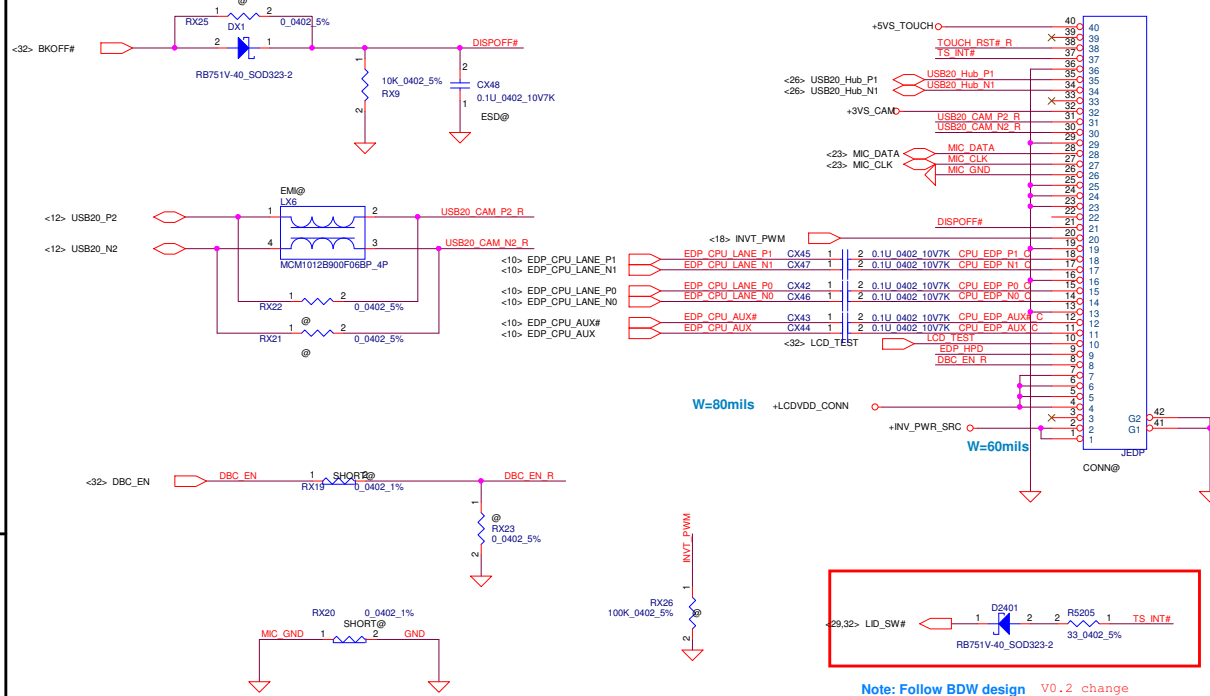
## LCD backlight PWR CTRL



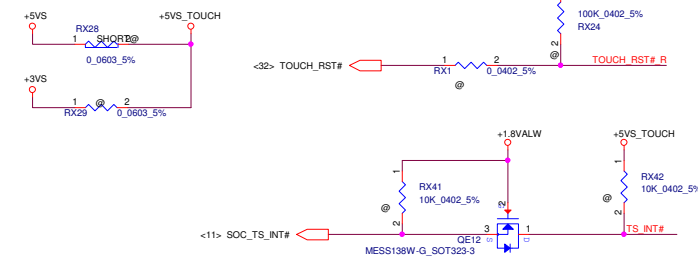
## Webcam PWR CTRL



## LCD Connector



## \* Touch Screen Panel

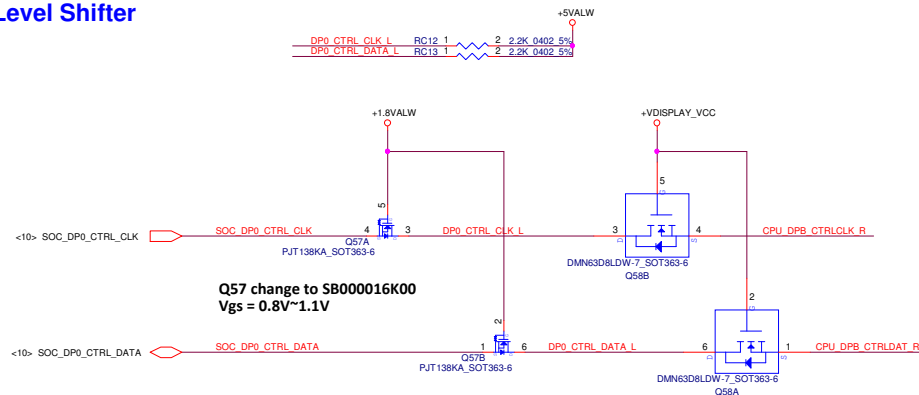
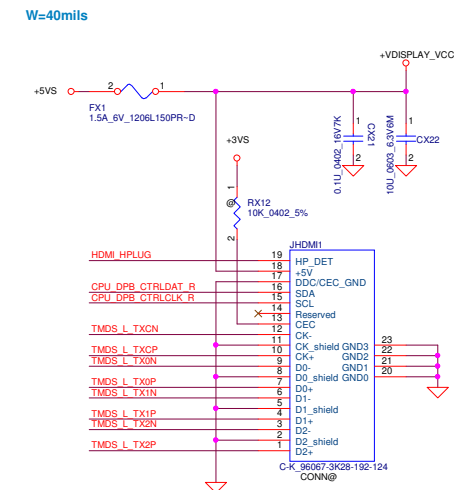
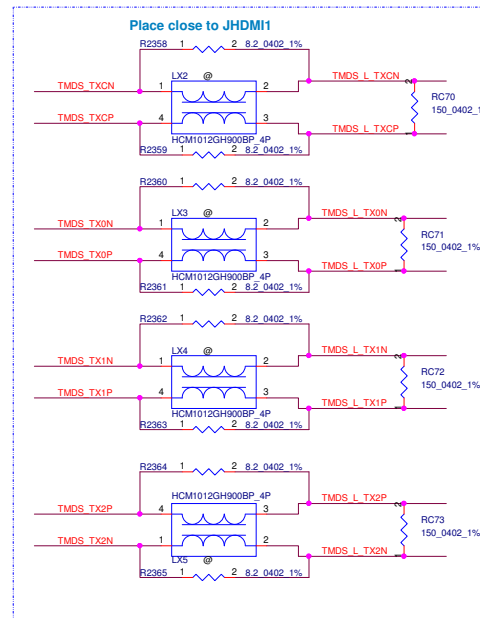
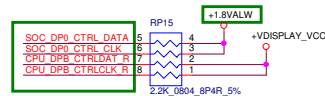
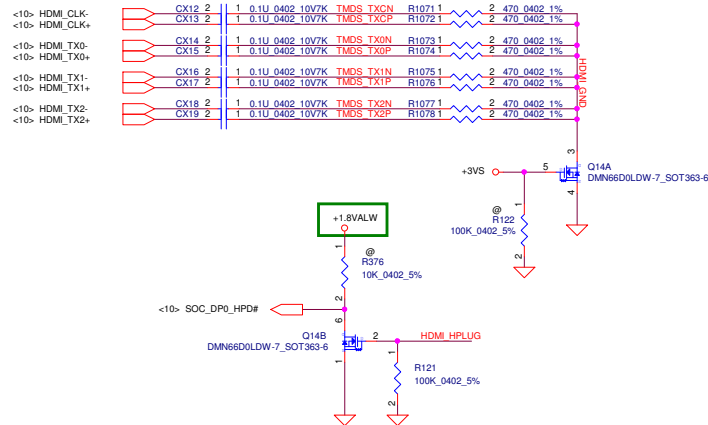


Closed to JEDP

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Date: Tuesday, June 16, 2015		Sheet	20 of 44

**Main Func = HDMI**

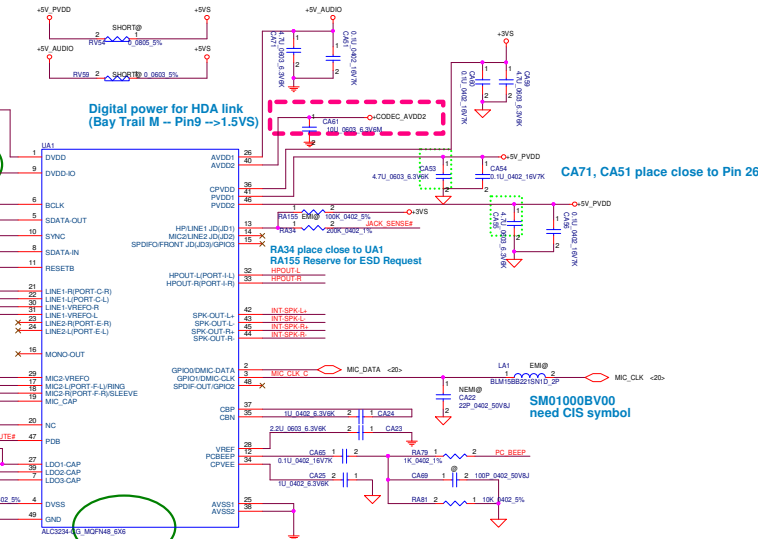
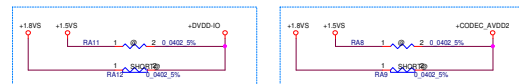
ROYALTY HDMI W/LOGO	
Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM



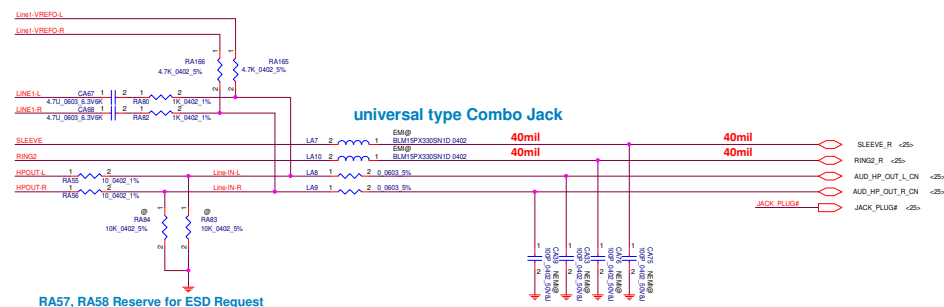
V0.2 change

Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> <b>P21-HDMI</b> Document Number <b>LA-C57P</b>	
Issued Date	2014/11/10	Deciphered Date	2015/11/25		
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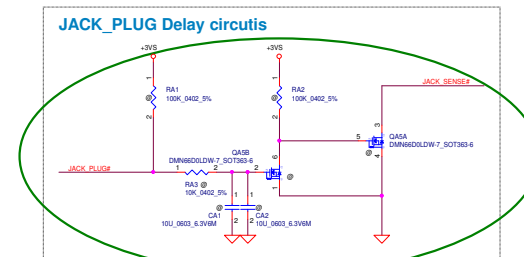




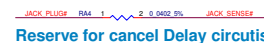
0724: change the cymbal to correct IC part and schematics



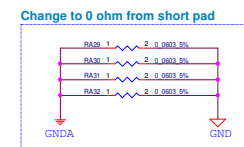
RA57, RA58 Reserve for ESD Request



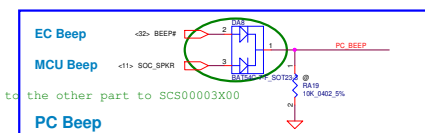
0721: pop all components for this portions



Reserve for cancel Delay circuitis

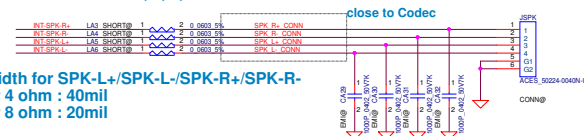


Place on the moat between GND & GNDA

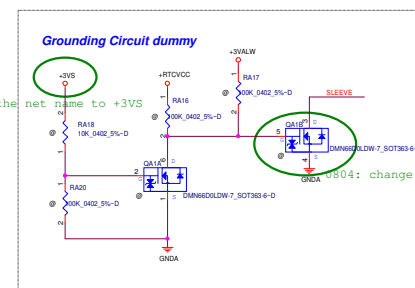


0718: change to the other part to SCS00003X00

Close to UA1  
Pin11,13,14,16



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-  
Speaker 4 ohm : 40mil  
Speaker 8 ohm : 20mil



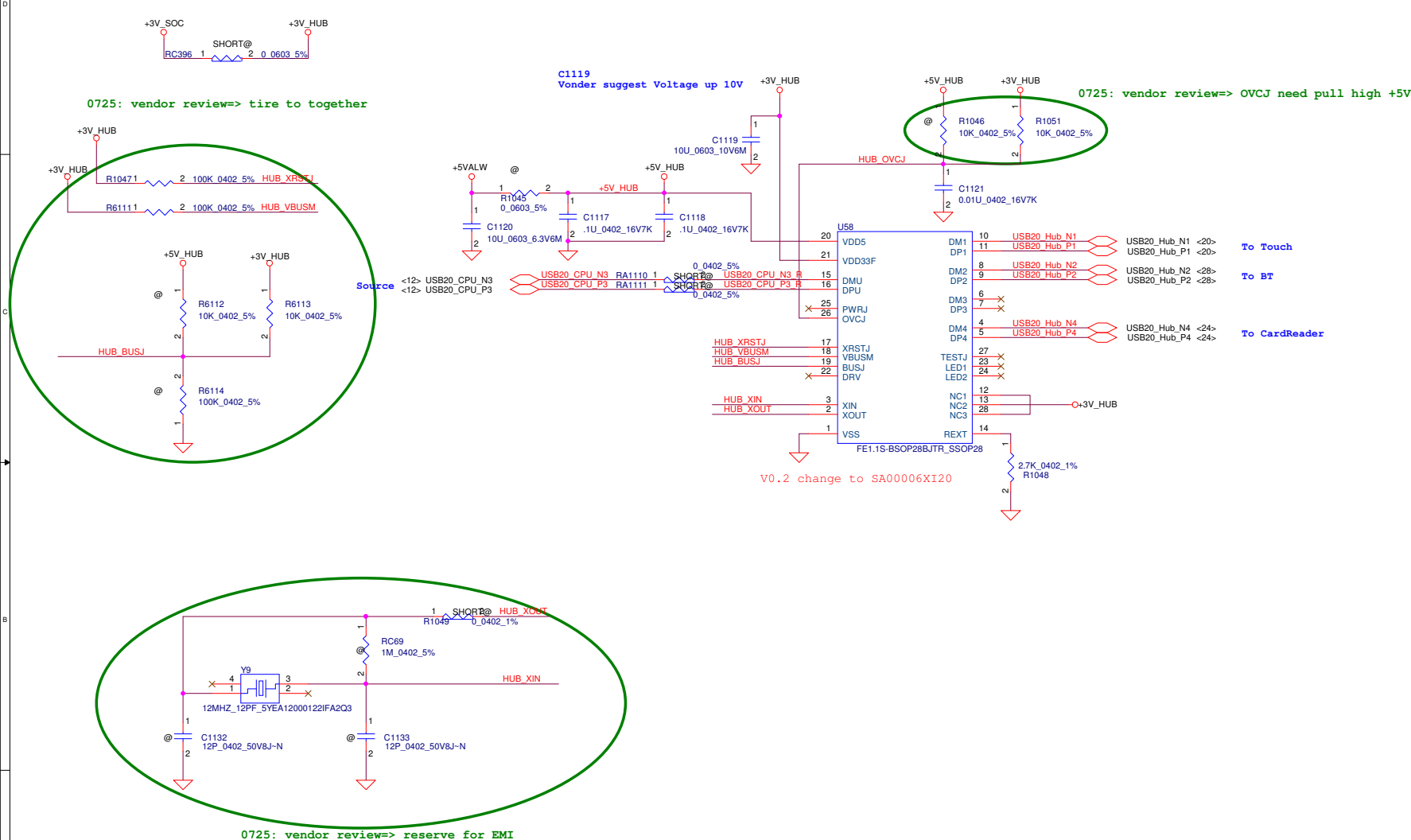
0718: change the

0804: change to the part name



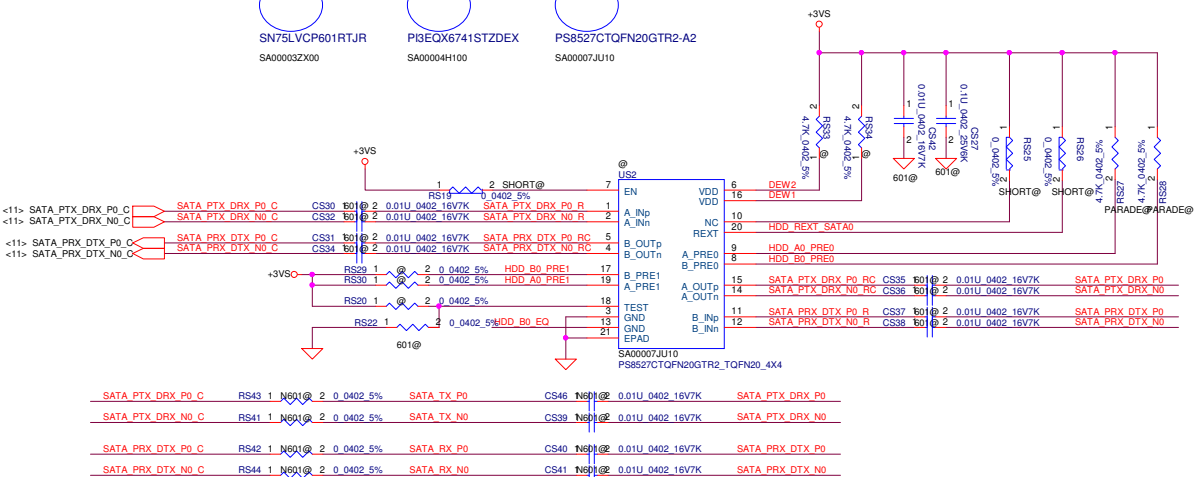


Main Func = HUB 2.0



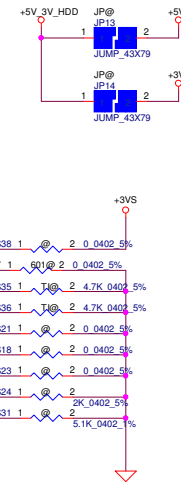
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Main Func = HDD

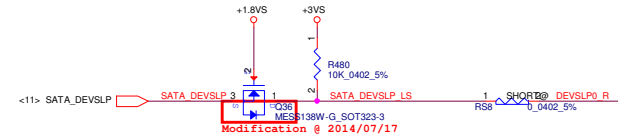
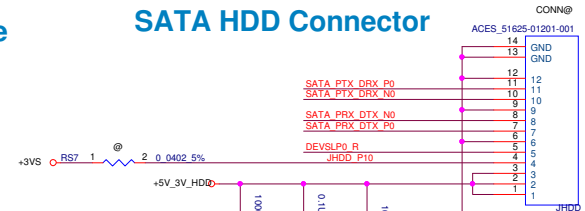


	DE	EQ
PARADE	-6dB	2.4dB
TI	-4dB	0dB

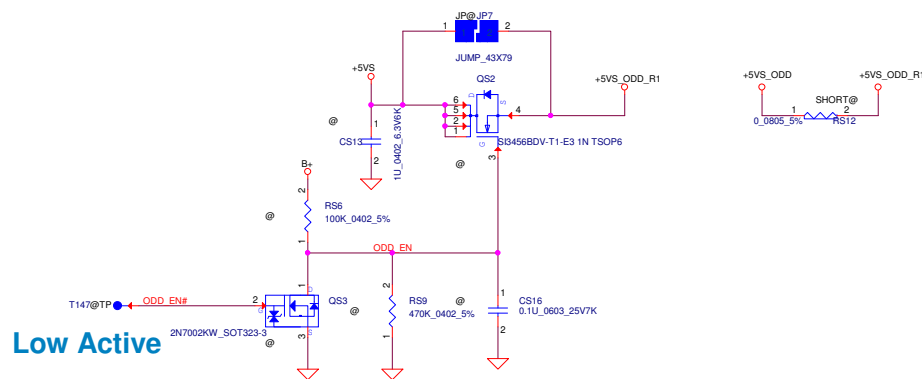
## +5V\_HDD Source



## SATA HDD Connector

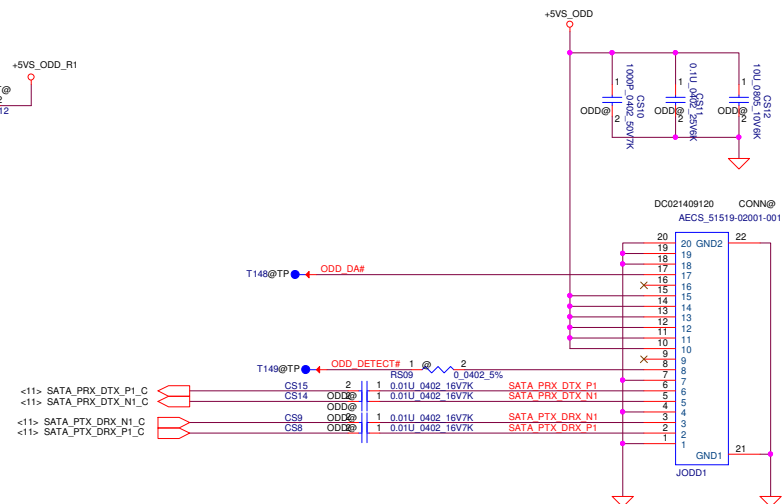


## ODD Power Control

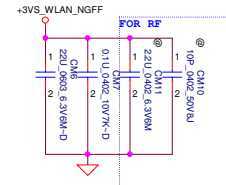
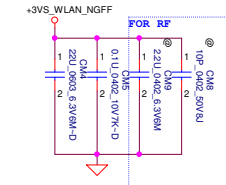
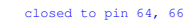
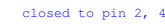
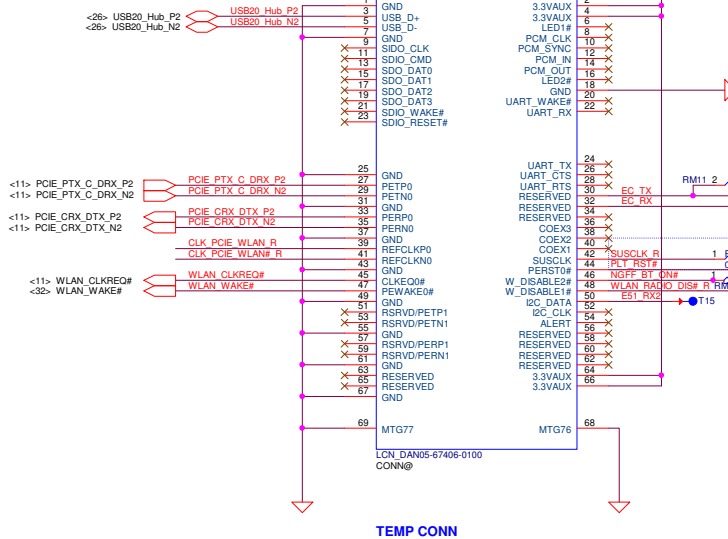
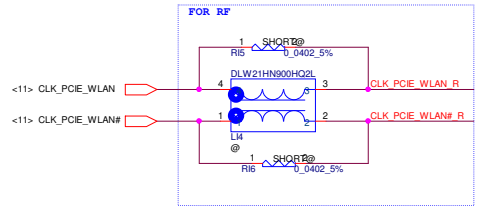
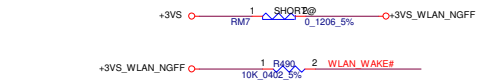


Low Active

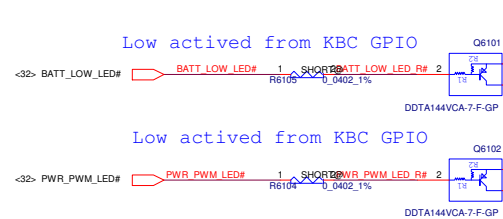
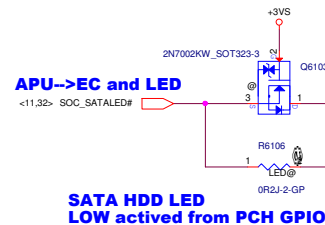
## SATA ODD Connector



**Main Func = NGFF**



```
0721: change power rail to +3VS_WLAN_NGFF
```

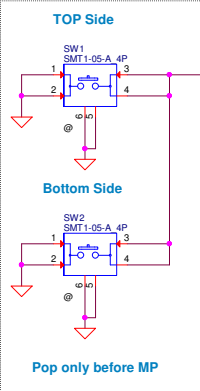


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				<i><b>LA-C57IP</b></i>	
				Date	Tuesday, June 16, 2015
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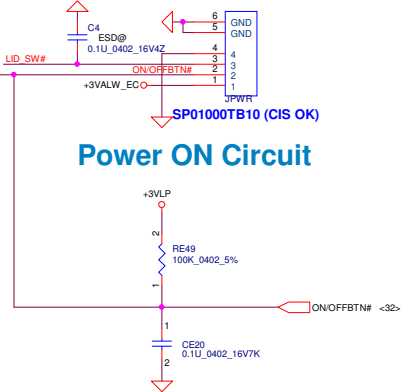
Main Func = Touch Pad

ON/OFF switch

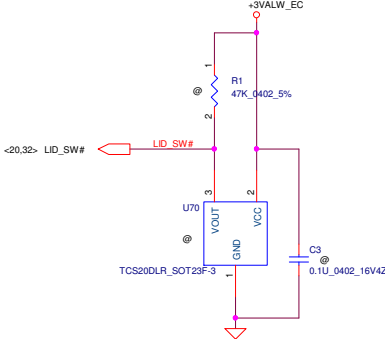


POWER/B

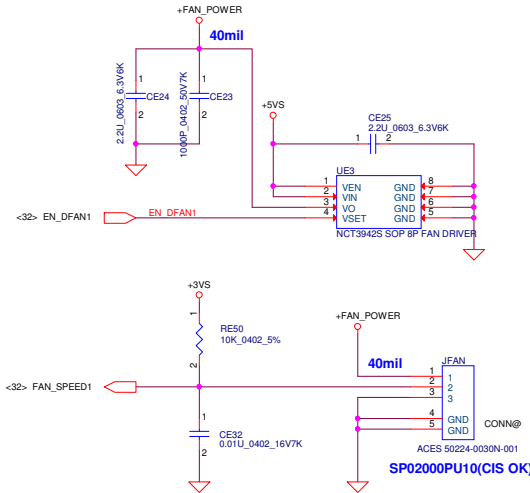
Power ON Circuit



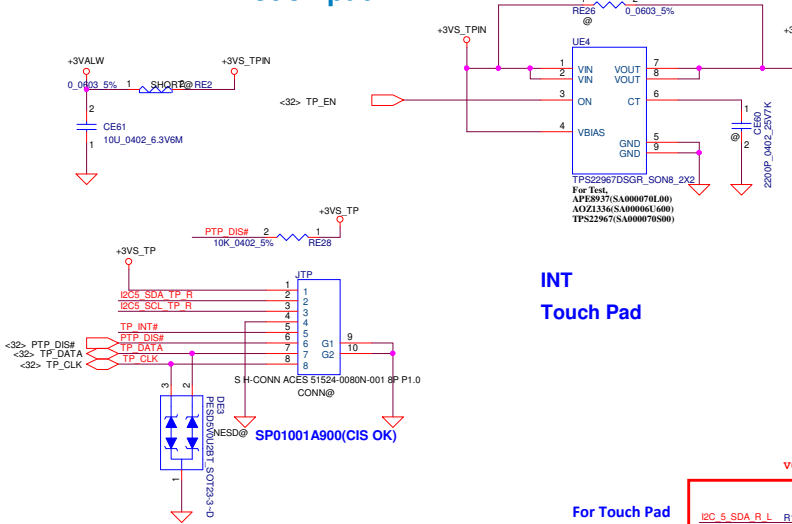
LID Switch



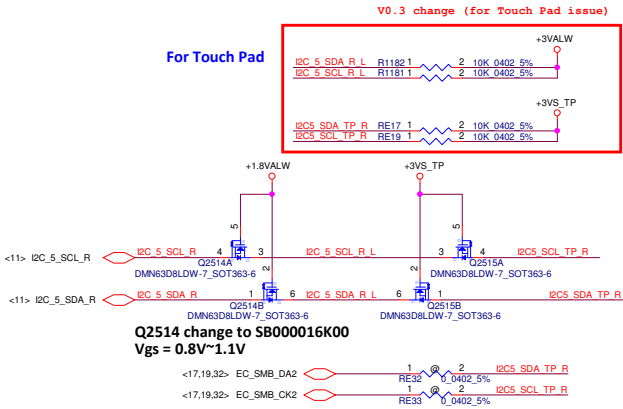
FAN Control circuit



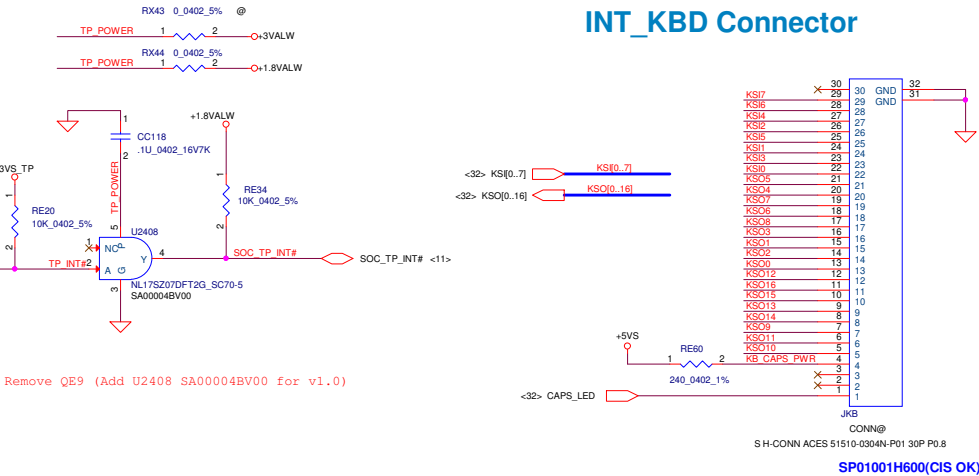
Touch pad



INT Touch Pad



INT\_KBD Connector

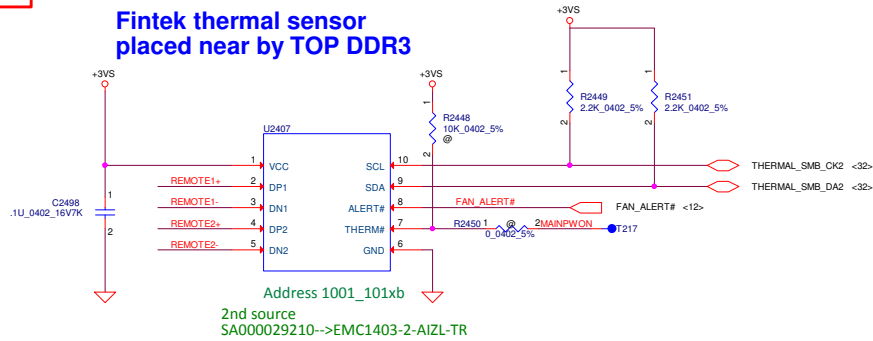


Event	PCH-TP_INT#	PCH-TP_INT#
S0	Interrupt	X
S3	X	Wake
1. Clamshell closed or Lid closed 2. Tablet mode for Convertible design 3. Disable TP function by ht-key	X	X

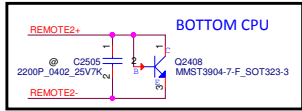
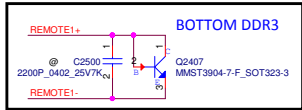
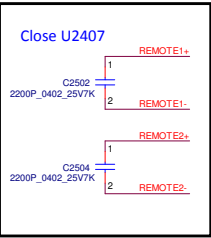


Main Func = Thermal

Fintek thermal sensor  
placed near by TOP DDR3



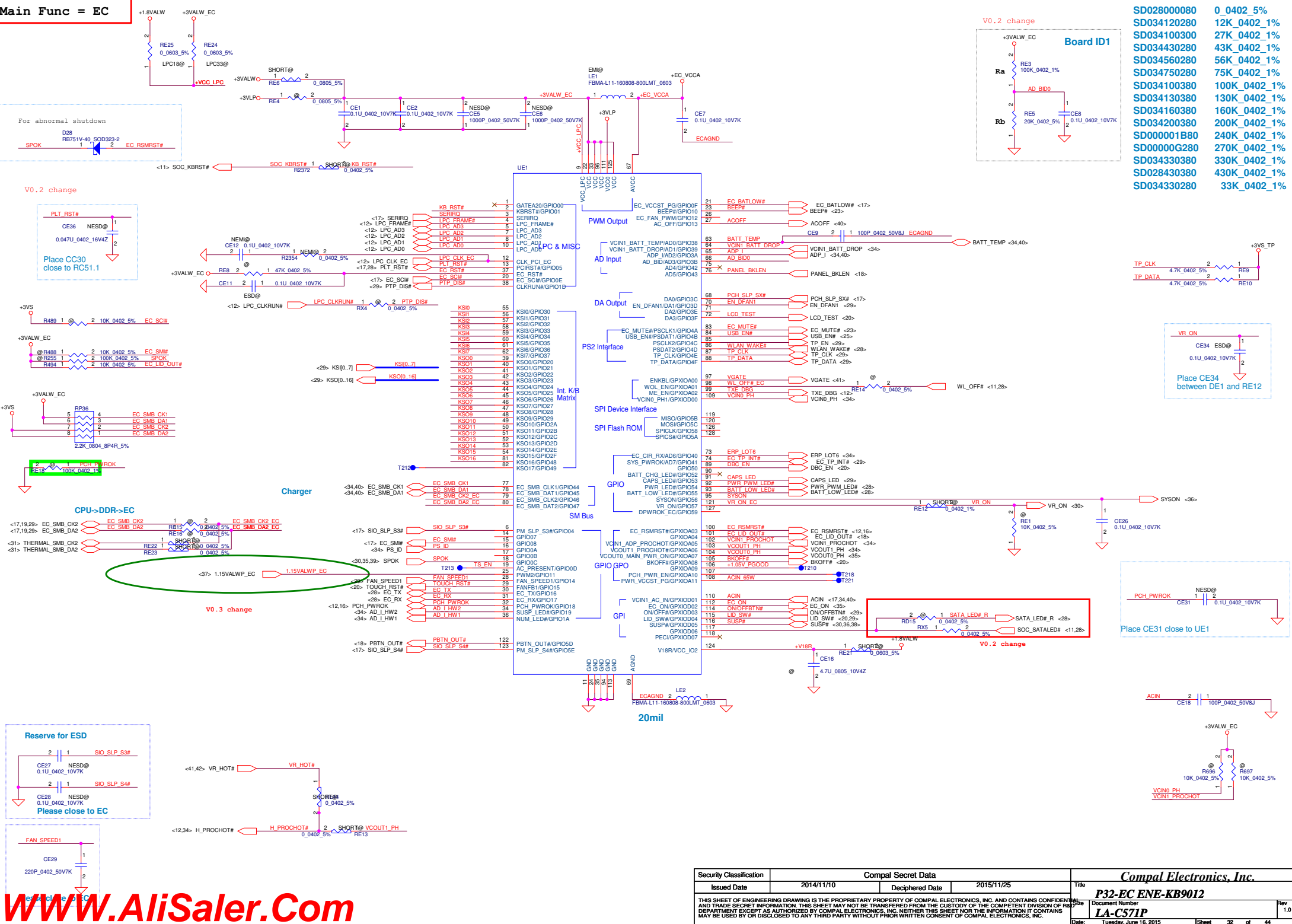
Address 1001\_101xb  
2nd source  
SA000029210-->EMC1403-2-AIZL-TR



REMOTE1,2 (+/-) :  
Trace width/space:10/10 mil  
Trace length:<8"

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Main Func = EC

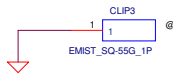
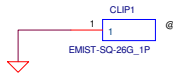
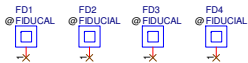
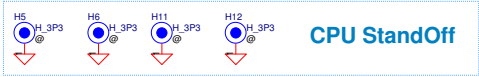
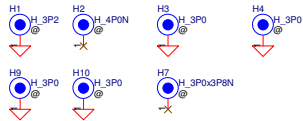


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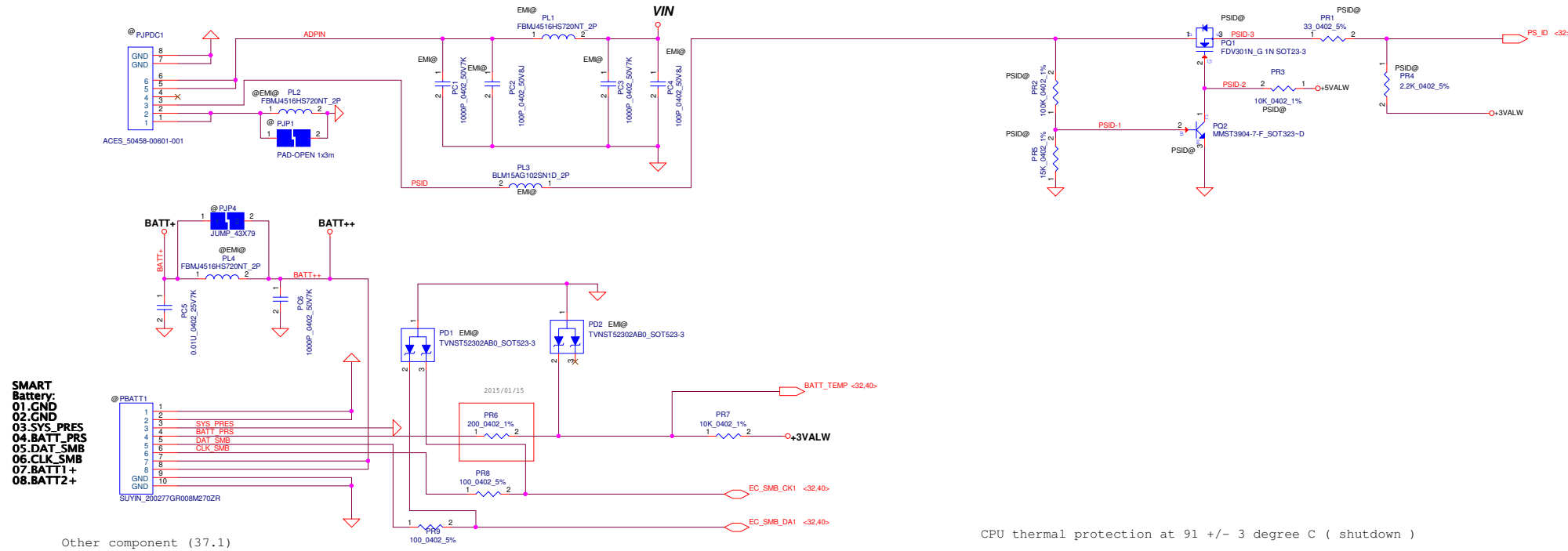
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Main Func = Screw Hole

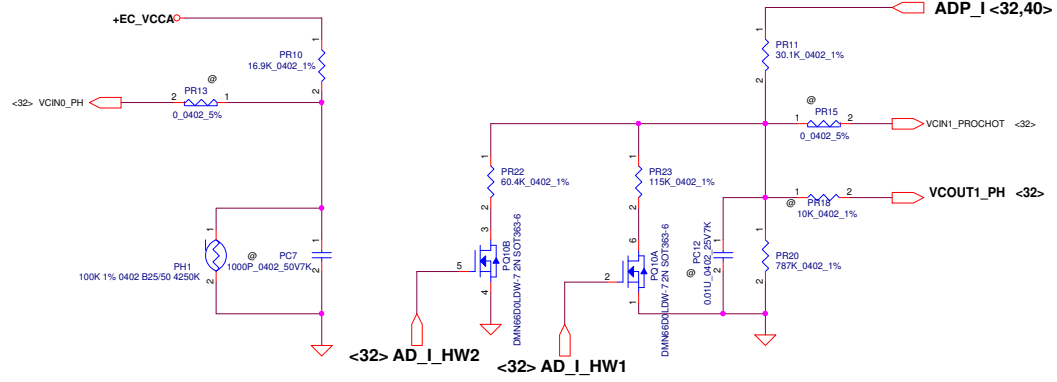
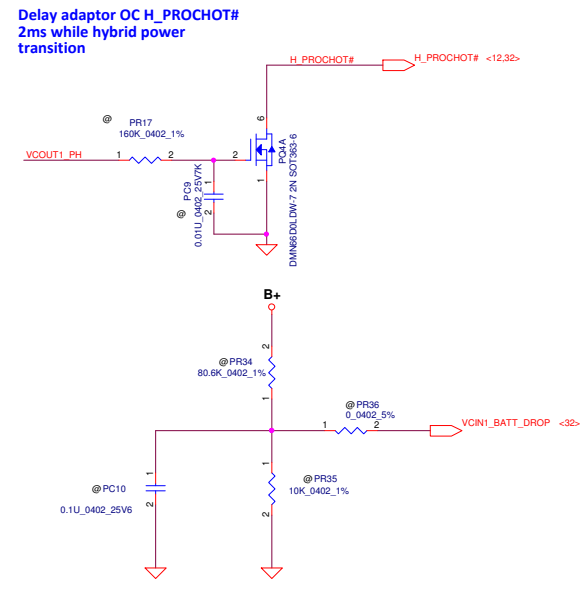
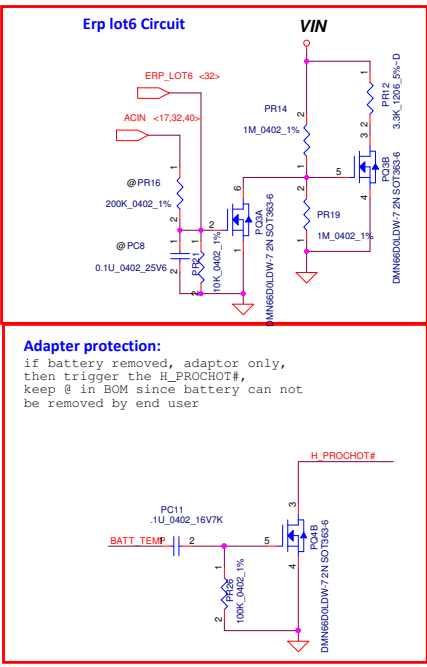
Screw Hole



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CPU thermal protection at 91 +/- 3 degree C ( shutdown )

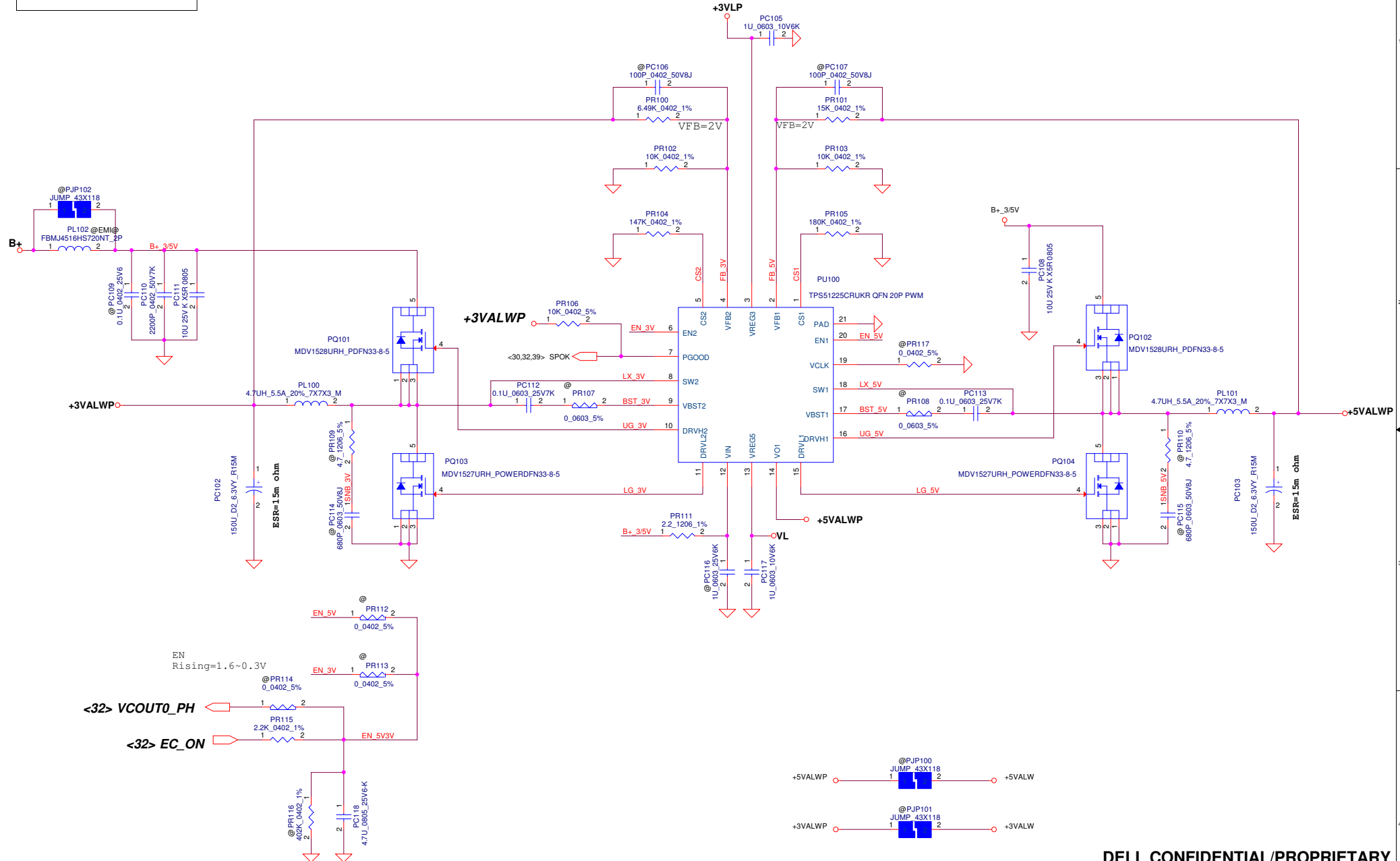


ADP\_I(with selector) to support "PWC" function.

H_PROCHOT#	AD_I_HW1	AD_I_HW2
35W	0	0
45W	1	0
55W	0	1
65W	1	1

3VALWP  
TDC 5.25A  
Peak Current 6.56A  
OCP current 8.53A

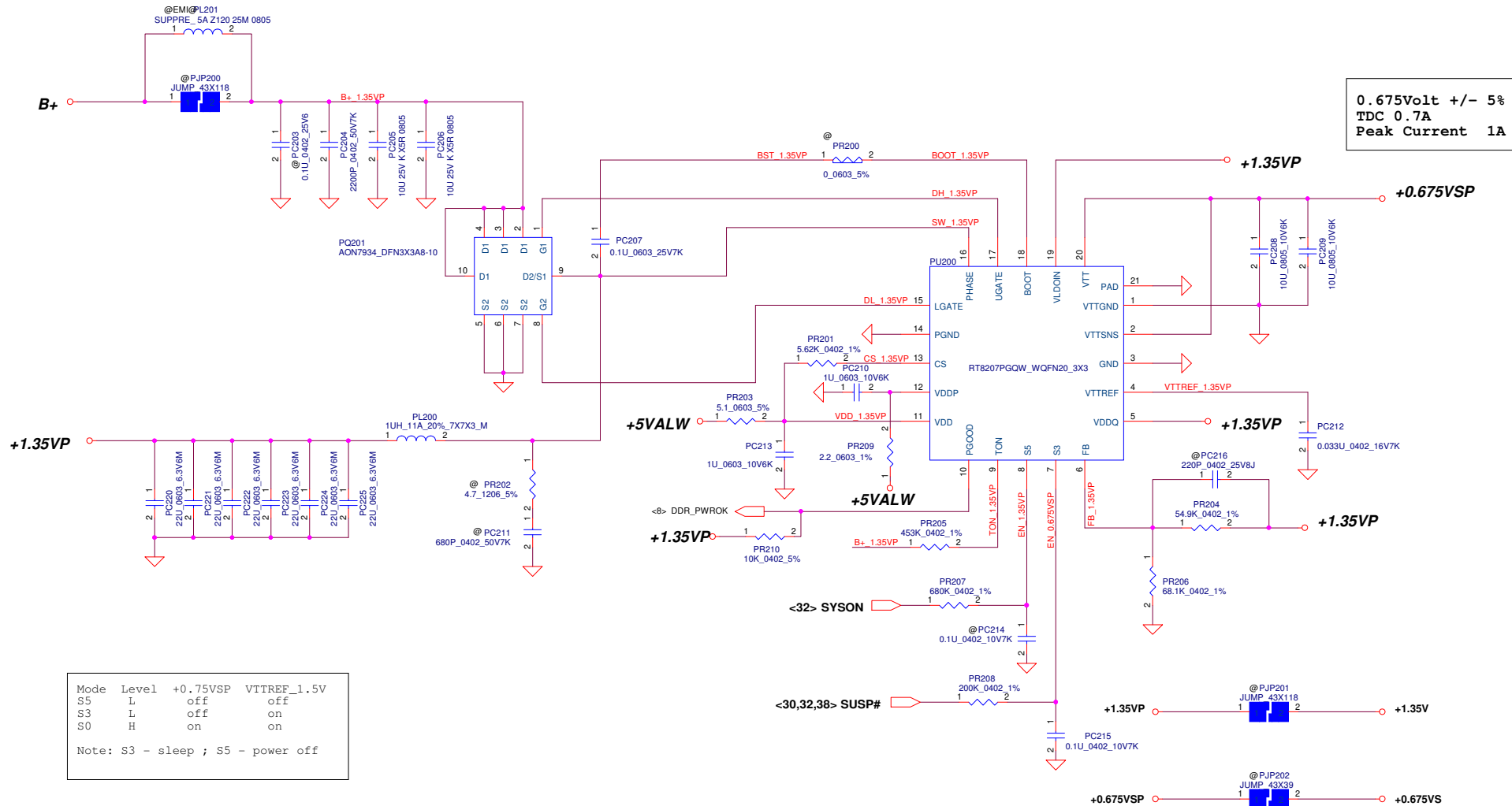
5VALWP  
TDC 5.3A  
Peak Current 6.62A  
OCP current 8.61A



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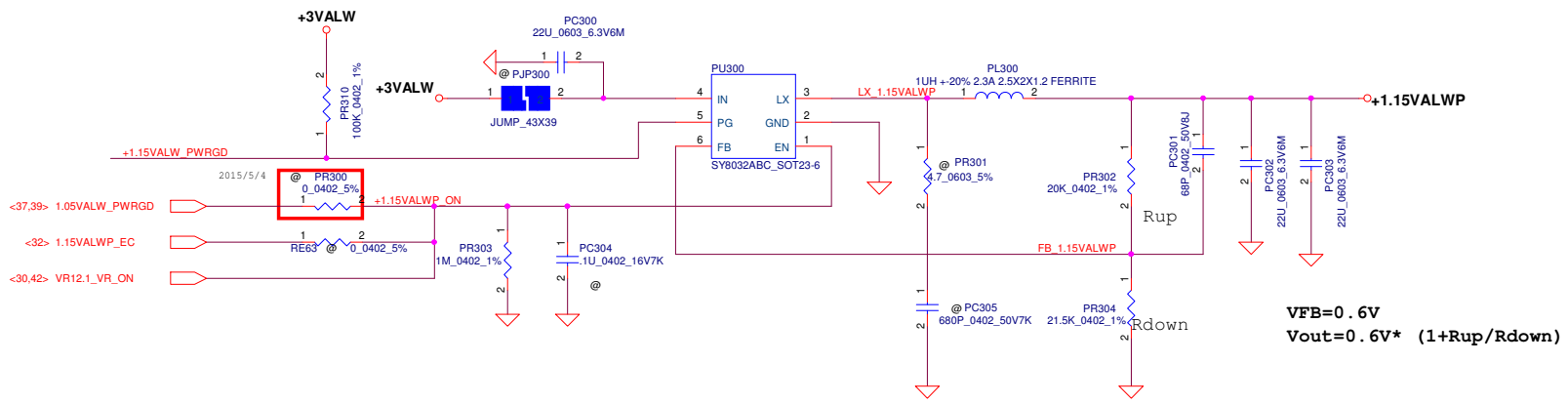
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1.35VP  
TDC 3.6A  
Peak Current 4.5A  
OCP current 6A



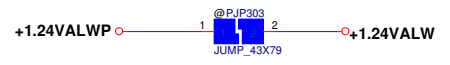
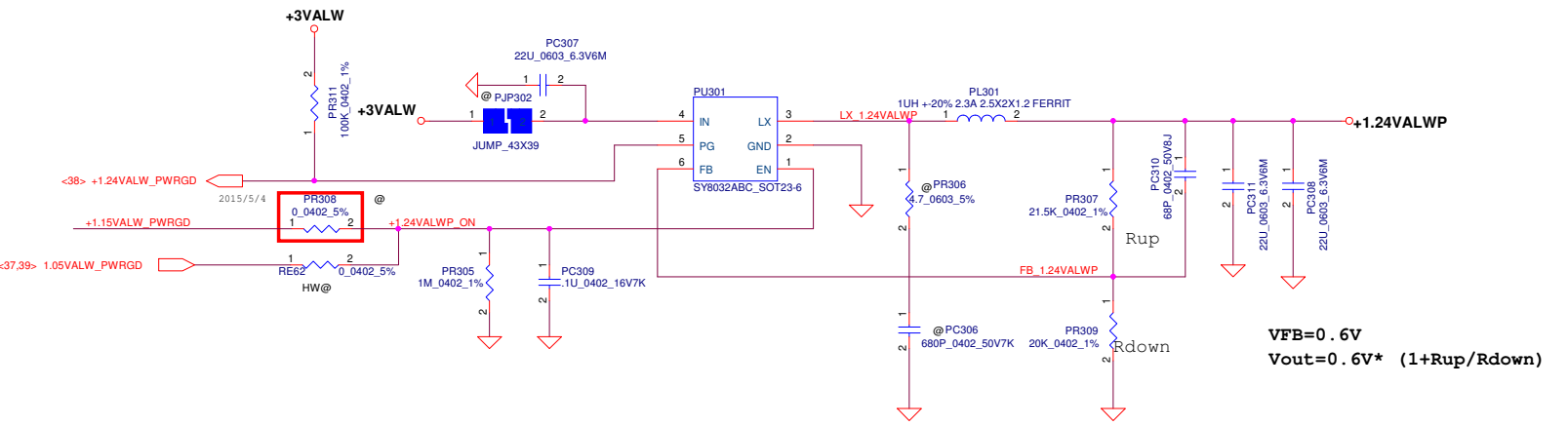
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**+1.15VALWP**  
TDC 0.64A  
Peak Current 0.8A  
OCP current 3.5A

$V_{FB}=0.6V$   
 $V_{out}=0.6V * (1+R_{up}/R_{down})$

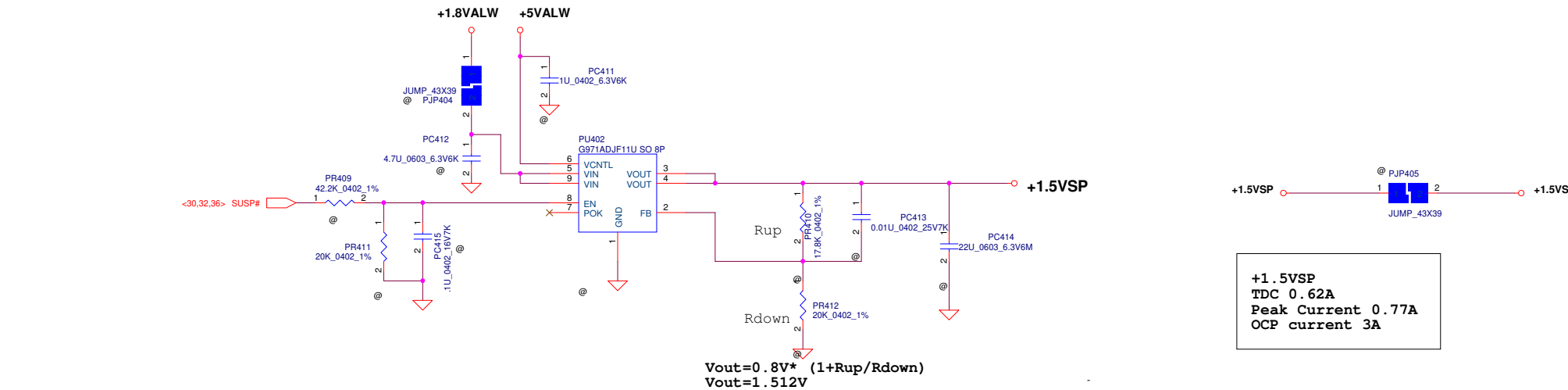
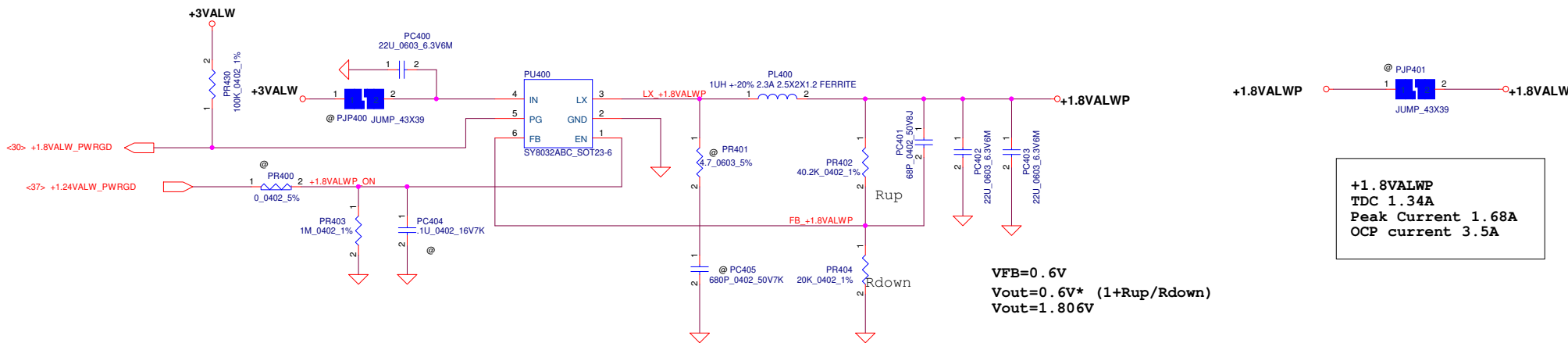


**+1.24VALWP**  
TDC 0.72A  
Peak Current 0.9A  
OCP current 3.5A

$V_{FB}=0.6V$   
 $V_{out}=0.6V * (1+R_{up}/R_{down})$

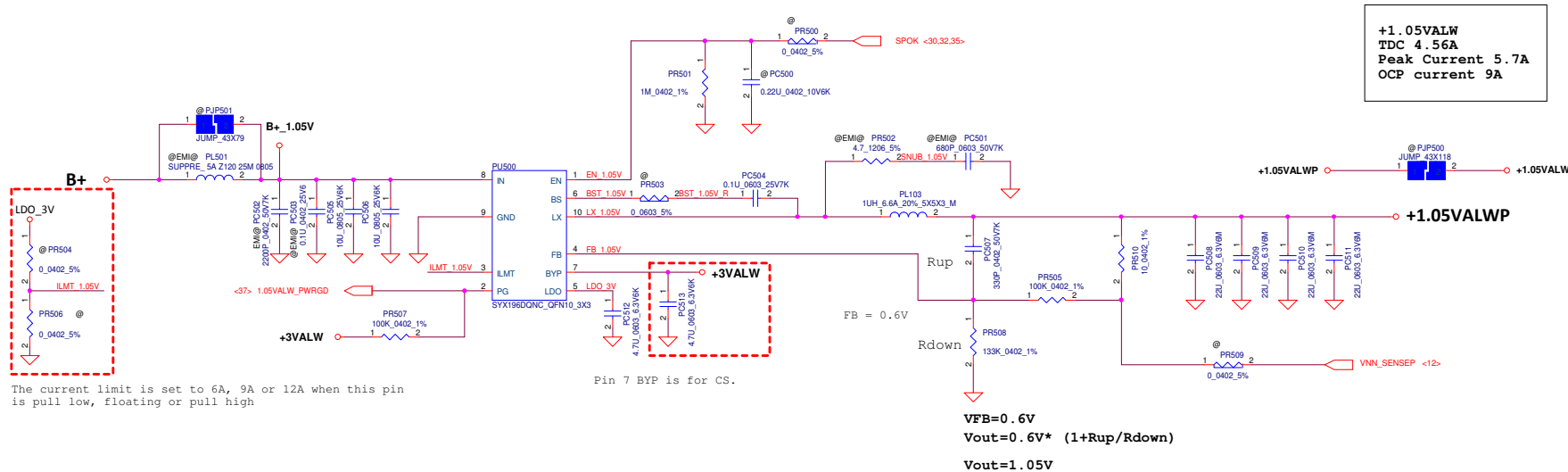
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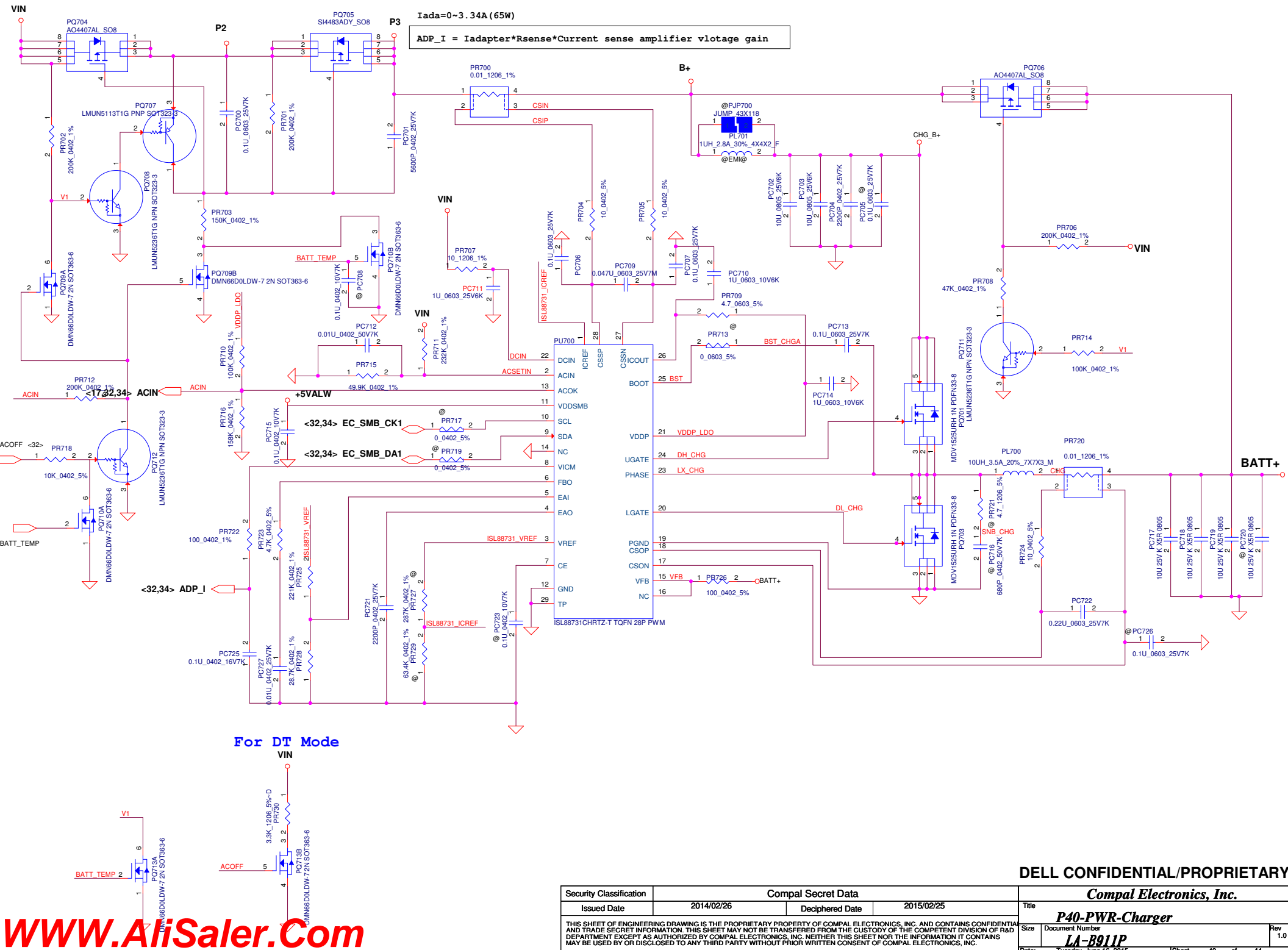
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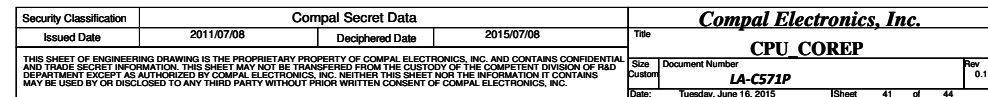
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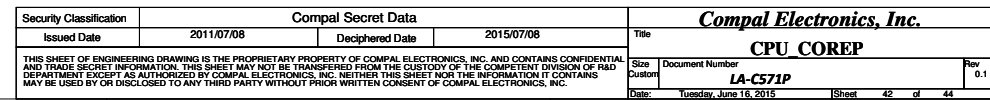


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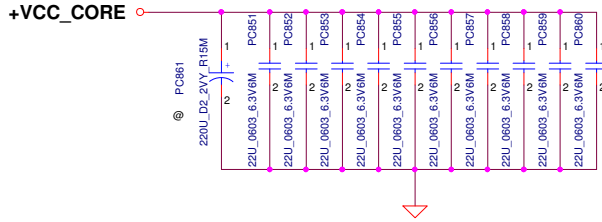
```
VCC_CORE
Peak Current 7.7A
OCP current 9.66A
```



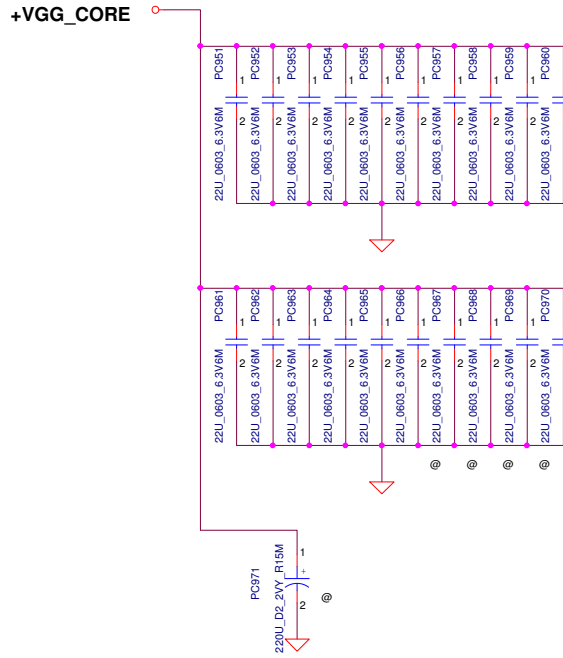
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VGG_CORE
Peak Current 11A
OCP current 15.18A
```



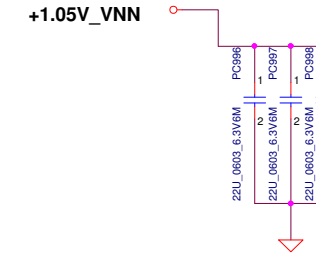
22U\_0603 \* 14 + reserved+220uF 15m ohm



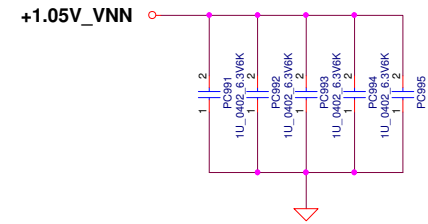
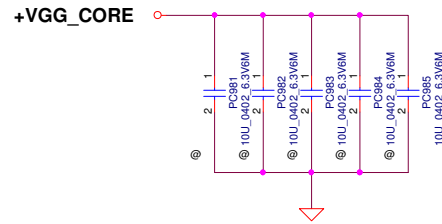
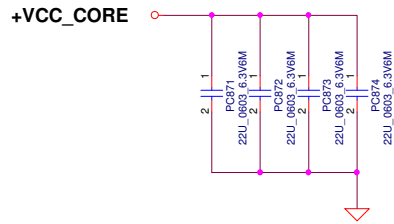
22U\_0603 \* 16 +4 reserved+220uF 15m ohm



22U\_0603 \* 3



Place on CPU Back Side.



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For PS2/PS3 ripple			PR829 change 976 from to 9.31Kohm , PR836 change 412 from to 4.02K ohm	15/01/15	EVT
2		For PS2/PS3 ripple			PR629 change 39.2k from to 48.9Kohm , PR636 change 14k from to 17.4K ohm , PC612 change form 470pF to 270pF	15/01/15	EVT
3		Compal ESD team request			PR6 change 100ohm from to 200 ohm	15/01/15	EVT
4		For HW power sequency			PR300 change to reserve	4/05/15	DVT2
5		For HW power sequency			PR308 change to reserve	4/05/15	DVT2
5							
6							
7							

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